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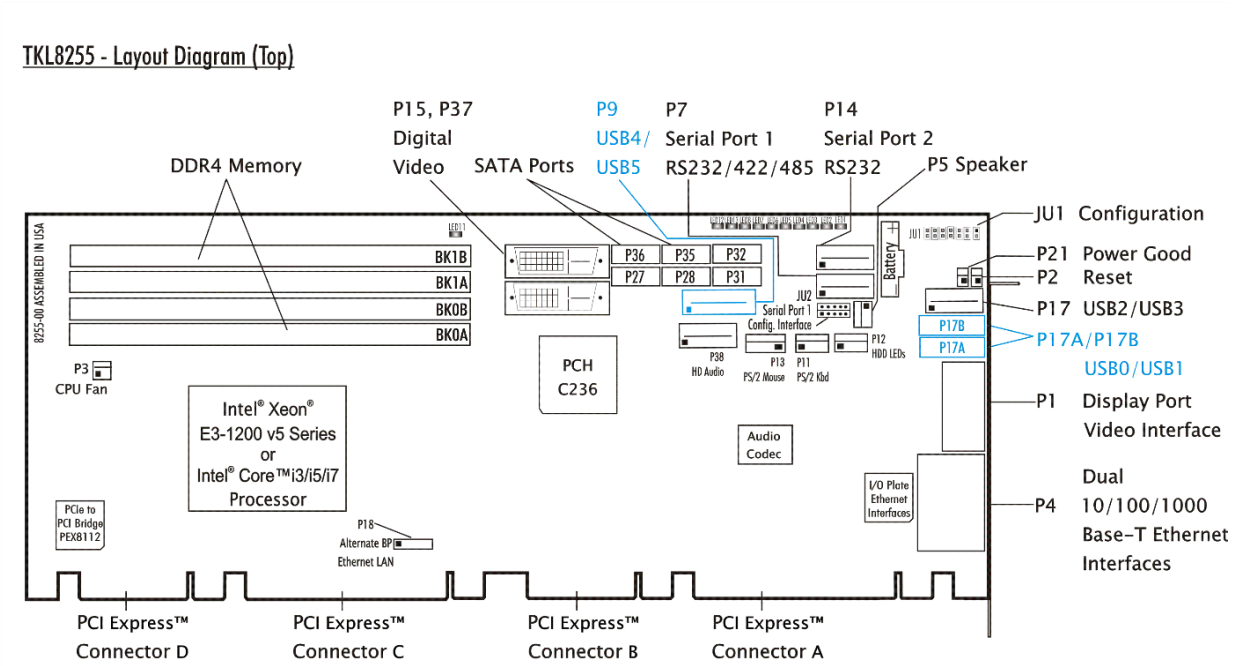
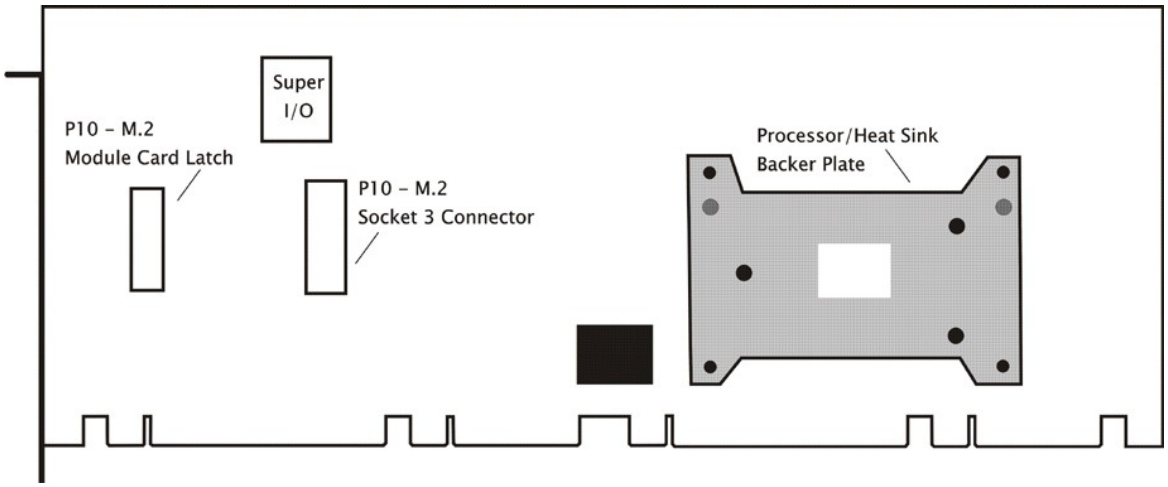
# Technical Information –Jumpers, Connectors and Memory
# TKL8255 (8255-xxx) Single-Processor, PICMG 1.3 System Host Board

## Layout Diagram – Top




## Layout Diagram – Bottom



## Jumpers

The setup of the configuration jumpers on the SHB is described below. An asterisk (*) indicates the default value of each jumper.

**NOTE:** Jumper JU1 is a dual-row, 14-pin jumper. Each position controls the operation of a specific SHB implementation

**NOTE:** For the three-position JU12 jumper, "RIGHT" is toward the I/O bracket side of the board; "LEFT" is toward the header connector P14.

**JU1 Pins 1-2 and 3-4** — **CMOS Clear**
Install on pins 1 and 2 to operate *
Install on pins 3 and 4 to clear.

**Note:** To clear the CMOS, power down the system and install the JU1 jumper on pins 3 and 4. Wait for at least two seconds, move the jumper back to pins 1 and 2 and turn the power on. Clearing CMOS on the TKL8255 will not result in a checksum error on the following boot. If you want to change a BIOS setting, you must press *DEL* or the *F2* key during POST to enter BIOS setup after clearing CMOS.

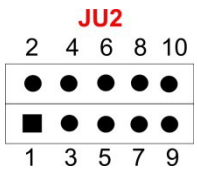
**JU1 Pins 5-6** — **Flash Descriptor Security Override**
No jumper installed on pins 5 and 6 is the normal SHB operating mode.*
Install jumper on pins 5 and 6 at power-on to override SPI-based write policies to unconditionally allow SPI updates.

**JU1 Pins 7-8** — **Clear Password**
No jumper installed on pins 7 and 8 is the normal SHB operating mode.*
Install jumper on pins 7 and 8 for one power-up cycle to reset the password to the default (null password).

**JU1 Pins 11-12** — **Management Engine (ME) Recovery**
No jumper installed on pins 11 and 12 is the normal SHB operating mode.*
Install a jumper on pins 11 and 12 at power-on to initiate ME recovery.

**JU1 Pins 13-14** — **XDP VCCST Override**
No jumper installed on pins 13 and 14 is the normal SHB operating mode.*
Installing a jumper on pins 13 and 14 supports XDP debugging in PCH Sleep States

**JU2** — **Serial Port 1 Interface Configuration**
JU2 uses five jumpers to allow serial port one to be configured as either a RS232 or a RS422/RS485 electrical interface. The jumper tables below illustrate the possible interface configurations for serial port one.




RS232 operation* – Jumper 1 to 2 **and** 3 to 4 **and** 9 to 10
RS485 Full Duplex, No Termination – Jumper 1 to 2 **and** 9 to 10[1]
RS485 Half Duplex, No Termination – Jumper 9 to 10
RS485 Full Duplex, With Termination – Jumper 1 to 2 **and** 5 to 6[2]
RS485 Half Duplex, With Termination – Jumper 5 to 6 **and** 9 to 10

Notes:
1 – Shut between pins 9 and 10 can optionally be removed to unconditionally enable the Tx driver
2 – Shut between pins 9 and 10 can optionally be installed to unconditionally enable the Tx driver

## Status LEDs

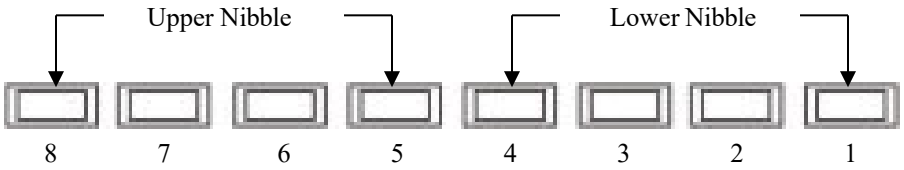
### POST Code LEDs 1 - 8

As the POST (Power On Self-Test) routines are performed during boot-up, test codes are displayed on Port 80 POST Code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LEDs are located on the top of the SHB, just above the board's SATA connectors and slightly toward the right. The POST Code LEDs and are numbered from right (position 1 = LED1) to left (position 8 – LED8). Refer to the board layout diagram for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. Specific test codes are listed in Appendix A - BIOS Messages section of the TKL8255 Technical Reference Manual. After a normal POST sequence, the LEDs are off (00h) indicating that the SHB's BIOS has passed control over to the operating system loader typically at interrupt INT19h. The chart is from Appendix A and can be used to interpret the LEDs into hexadecimal format during POST.

| Upper Nibble (UN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED8 | LED7 | LED6 | LED5 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |

| Lower Nibble (LN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED4 | LED3 | LED2 | LED1 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |




**TKL8255 POST Code LEDs**

## P4A/P4B Ethernet LEDs

The I/O bracket houses the two RJ-45 network connectors for Ethernet LAN1 and LAN2. Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

| LED/Connector | Description |
|---|---|
| Activity LED | This LED identifies the validity of a link on the specific interface. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets). |
| Off | No valid link exists on this interface. |
| On (flashing) | Indicates network transmit or receive activity. |
| On (solid) | Indicates a valid link with no transmit or receive activity. |
| Speed LED | This multi-color LED identifies the connection speed of the SHB's P4A (LAN2) and P4B (LAN1) Ethernet interfaces. These are the lower LEDs on the dual LAN connector (i.e., toward the edge connectors). |
| Green | Indicates a valid link at 1000-Mb/s or 1Gb/s |
| Orange | Indicates a valid link at 100-Mb/s. |
| Off | Indicates a valid link at 10-Mb/s |
| RJ-45 Network Connectors | The RJ-45 network connector requires a Connectors category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection. |

## LED11 - Backplane LAN LED

LED11 is located just above the right side of memory DIMM connector BK1B. A flashing LED11 indicates that network transmit and receive activity is occurring on the Ethernet LAN routed to the board's edge connector C / cable connector P18. This LAN provides a network interface for use on a compatible PICMG 1.3 backplane or over a cable.

## LED12 generally indicates a CAT Error, and here is a quick guide to the blink rates:

- THERMTRIP: on 2 sec/off 2 sec
- CATERR: 2 blinks/2 secs
- IMVP8_VR_FAULT: 1 blink/2 sec (vccore/vgt regulator fail after startup)
- PS_PWROK & PLT_RESET# not asserted: on solid (startup issue)

## LED13 – M.2 Activity LED

LED13 is located on the rear of the SHB, near the M.2 slot. A flashing LED13 indicates that I/O activity is occurring on the M.2 bus.

# Connectors

**NOTE:**
A connector's square solder pad located on the bottom side of the PCB indicates pin 1.

### P1 –DisplayPort Connector

20-pin digital A/V interface,
Molex #105020-001

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | TXP0 | 13 | GND |
| 2 | GND | 14 | GND |
| 3 | TXN0 | 15 | AUX_P |
| 4 | TXP1 | 16 | GND |
| 5 | GND | 17 | AUX_N |
| 6 | TXN1 | 18 | HPDET |
| 7 | TXP2 | 19 | GND |
| 8 | GND | 20 | VCC3 DP |
| 9 | TXN2 | 21 | SGGND1 |
| 10 | TXP3 | 22 | SGGND2 |
| 11 | GND | 23 | SGGND3 |
| 12 | TXN3 | 24 | SGGND4 |

### P2 - Reset Connector

2 pin single row header, Amp #640456-2

| PIN | SIGNAL |
|---|---|
| 1 | Gnd |
| 2 | Reset In |

### P3 – CPU Fan Power Connector

4 pin single row MTA, Molex #47053-1000

| PIN | SIGNAL |
|---|---|
| 1 | Gnd |
| 2 | +12V |
| 3 | Fan Tach |
| 4 | PWM Control Signal |

### P4A/P4B – Dual 10/100/1000Base-T Ethernet Connector - LAN1 and LAN2

RJ-45/Dual connector, Pulse #JG0-0024NL
Each individual RJ-45 connector is defined as follows:

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1A | L2_MDI0n | 1B | L1_MDI0n |
| 2A | L2_MDI0p | 2B | L1_MDI0p |
| 3A | L2_MDI1n | 3B | L1_MDI1n |
| 4A | L2_MDI1p | 4B | L1_MDI1p |
| 5A | L2_MDI2n | 5B | L1_MDI2n |
| 6A | L2_MDI2p | 6B | L1_MDI2p |
| 7A | L2_MDI3n | 7B | L1_MDI3n |
| 8A | L2_MDI3p | 8B | L1_MDI3p |
| 9A | VCC_1.8V | 9B | VCC_1.8V |
| 10A | GND_A | 10B | GND_b |

Notes:
1 – LAN ports support standard CAT5 Ethernet cables
2 – P4A is LAN2 and P4B is LAN1

### P5 - Speaker Port Connector

4 pin single row header, Amp #640456-4

| PIN | SIGNAL |
|---|---|
| 1 | Speaker Data |
| 2 | NC |
| 3 | Gnd |
| 4 | +5V |

## Connectors (continued)

### P7 – Serial Port 1 Connector – RS422/RS485 Full Duplex Connections

10 pin dual row header, Amp #5103308-1

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | Carrier Detect | 2 | Data Set Ready-I |
| 3 | Receive Data-I | 4 | Request to Send-O |
| 5 | Transmit Data-O | 6 | Clear to Send |
| 7 | Data Terminal Ready-O | 8 | Ring Indicator-I |
| 9 | Gnd | 10 | NC |

Note: See JU2 pin-puts listed in the Jumpers & LEDs section on this document to enable serial port 1 signal connections.

### P9 – Dual Universal Serial Bus (USB) 3.0 Connector

19 pin dual row header, Lotes ABA-USB-152-K04
(+5V fused with self-resetting fuse)

| PIN | USB4 SIGNAL | PIN | USB5 SIGNAL |
|---|---|---|---|
| 1 | +5V-USB4 | 11 | USBP5P |
| 2 | USB3_RX5AN | 12 | USBP5N |
| 3 | USB3_RX5AP | 13 | GND |
| 4 | GND | 14 | USB3_TX6BP |
| 5 | USB3_TX5BN | 15 | USB3_TX6BN |
| 6 | USB3_TX5BP | 16 | GND |
| 7 | GND | 17 | USB3_RX6AP |
| 8 | USBP4N | 18 | USB_RX6AN |
| 9 | USBP4P | 19 | +5V-USB5 |
| 10 | ID | | |

### P10 – M.2 M-Key Slot (SHB bottom side)

74 pin, JAE Electronic SM3ZS067U410AMR1000

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | GND | 2 | 3.3V |
| 3 | GND | 4 | 3.3V |
| 5 | M2_PE_RXN3 | 6 | NC |
| 7 | M2_PE_RXP3 | 8 | NC |
| 9 | GND | 10 | SSD LED# |
| 11 | M2_PE_TXN3 | 12 | GND |
| 13 | M2_PE_TXP3 | 14 | GND |
| 15 | GND | 16 | GND |
| 17 | M2_PE_RXN2 | 18 | GND |
| 19 | M2_PE_RXP2 | 20 | NC |
| 21 | GND | 22 | NC |
| 23 | M2_PE_TXN2 | 24 | NC |
| 25 | M2_PE_TXP2 | 26 | NC |
| 27 | GND | 28 | NC |
| 29 | M2_PE_RXN1 | 30 | NC |
| 31 | M2_PE_RXP1 | 32 | NC |
| 33 | GND | 34 | NC |
| 35 | M2_PE_TXN1 | 36 | NC |
| 37 | M2_PE_TXP1 | 38 | M2_DEVSLP |
| 39 | GND | 40 | NC |
| 41 | M2_PE_RXP0 | 42 | NC |
| 43 | M2_PE_RXN0 | 44 | NC |
| 45 | GND | 46 | NC |
| 47 | M2_PE_TXN0 | 48 | NC |
| 49 | M2_PE_TXP0 | 50 | IO_RESET# |
| 51 | GND | 52 | M2SSD_CLKREQ |
| 53 | M2_CLK100N | 54 | PCH WAKE# |
| 55 | M2_CLK100P | 56 | NC |
| 57 | GND | 58 | NC |
| 67 | NC | 68 | PCH_SUSCLK |
| 69 | M2_PEDET | 70 | 3.3V |
| 71 | GND | 72 | 3.3V |
| 73 | GND | 74 | 3.3V |
| 75 | GND | | |

## Connectors (continued)

### P11 – PS/2 Keyboard Header

5 pin single row header, Amp #640456-5

| PIN | SIGNAL |
|---|---|
| 1 | Kbd Clock |
| 2 | Kbd Data |
| 3 | NC |
| 4 | Kbd Gnd |
| 5 | Kbd Power (+5V fused) with self resetting fuse |

### P12 – Hard Drive LED Connector

4 pin single row header, Amp #640456-4

| PIN | SIGNAL |
|---|---|
| 1 | LED + |
| 2 | LED - |
| 3 | LED - |
| 4 | LED + |

### P13 – PS/2 Mouse Header

6 pin single row header, Amp #640456-6

| PIN | SIGNAL |
|---|---|
| 1 | Ms Data |
| 2 | NC |
| 3 | Gnd |
| 4 | Ms Power (+5V fused) with self resetting fuse |
| 5 | Ms Clock |
| 6 | NC |

### P14 – Serial Port 2 Connector – RS232 Connections

10 pin dual row header, Amp #5103308-1

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | Carrier Detect | 2 | Data Set Ready-I |
| 3 | Receive Data-I | 4 | Request to Send-O |
| 5 | Transmit Data-O | 6 | Clear to Send |
| 7 | Data Terminal Ready-O | 8 | Ring Indicator-I |
| 9 | Gnd | 10 | NC |

Contact Trenton Systems support for specific application information on Serial Port 2 (P14).

### P15, P37 – Digital Video Connector (DVI-D)

24-socket digital video connector, Molex #0743205004

| PIN | SIGNAL | PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|---|---|
| 1 | DVI_TX2N | 9 | DVI_TX1N | 17 | DVI_TX0N |
| 2 | DVI_TX2P | 10 | DVI_TX1P | 18 | DVI_TX0P |
| 3 | Gnd | 11 | Gnd | 19 | Gnd |
| 4 | NC | 12 | NC | 20 | NC |
| 5 | NC | 13 | NC | 21 | NC |
| 6 | DVI_SCLK | 14 | 5V | 22 | Gnd |
| 7 | DVI_SDAT | 15 | Gnd | 23 | DVI_TXCP |
| 8 | NC | 16 | DVI_HPD | 24 | DVI_TXCN |

Note: Video connector supports standard DVI-D digital video cables

### P17A, P17B – Universal Serial Bus (USB) 3.0 Connectors (I/O Bracket)

USB vertical connectors, Molex #48404-0003
(+5V fused with self-resetting fuse)

| PIN | P17A SIGNAL | PIN | P17B SIGNAL |
|---|---|---|---|
| 1 | +5V-USB0 | 1 | +5V-USB1 |
| 2 | USB0- | 2 | USB1- |
| 3 | USB0+ | 3 | USB1+ |
| 4 | GND | 4 | GND |
| 5 | USB3_RX1AN | 5 | USB3_RX2AN |
| 6 | USB3_RX1AP | 6 | USB3_RX2AP |
| 7 | GND | 7 | GND |
| 8 | USB3_TX1BN | 8 | USB3_TX2BN |
| 9 | USB3_TX1BP | 9 | USB3_TX2BP |

Note: P17A is USB0 and P17B is USB1

## Connectors (continued)

### P18 - 10/100/1000Base-T Ethernet Connector – Alternate Backplane LAN Over Cable

8 pin single row connector, Molex #0554500859

| PIN | SIGNAL |
|---|---|
| 1 | A_MDI2N |
| 2 | A_MDI2P |
| 3 | A_MDI3N |
| 4 | A_MDI3P |
| 5 | A_MDI1N |
| 6 | A_MDI1P |
| 7 | A_MDI0N |
| 8 | A_MDI0P |

**BP LAN Cable Option**
You may elect to create your own backplane LAN cable using the mating Molex connector information below. However, Trenton does offer a pre-made alternate backplane LAN cable with the mating Molex connector on one end and an RJ45 connector mounted into an I/O bracket on the other end. The Trenton part number for the alternate backplane LAN cable is:**193500001150-00**.

*Note: Using the alternate backplane LAN cable effectively disconnects the LAN routing down to SHB edge connector C.*

Note:
The mating Molex connector to use when making this alternative Ethernet cable has a Molex part number of 0513360810.

### P21 – Power Good LED

2 pin single row header, Amp #640456-2

| PIN | SIGNAL |
|---|---|
| 1 | LED - |
| 2 | LED + |

### P27, P28, P31, P32, P35, P36 – SATA III 600 Ports

7 pin vertical locking connector, Molex #67800-8005

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | Gnd | 5 | RX- |
| 2 | TX+ | 6 | RX+ |
| 3 | TX- | 7 | Gnd |
| 4 | Gnd | | |

Notes:
1 – P27 = SATA0 interface, P28 = SATA1 interface,
P31 = SATA2 interface, P32 = SATA3 interface,
P35 = SATA4 interface, P36 = SATA5 interface,
2 – SATA connectors support standard SATA interface cables
3 – All SATA ports support SATA 3.0, SATA 2.0 and SATA 1.0 devices
4 – SATA 3.0 = 600MB/s data transfers, SATA 2.0 = 300MB/s data transfers and SATA 1.0 = 150MB/s data transfers

### P38 –HD Audio Connector – Audio Connections

10 pin dual row header, Amp #5103308-1

| PIN | SIGNAL | PIN | SIGNAL |
|---|---|---|---|
| 1 | Line In L | 2 | Line In R |
| 3 | GND | 4 | GND |
| 5 | Mic L | 6 | Mic R |
| 7 | GND | 8 | Sense_A |
| 9 | Line Out L | 10 | Line Out R |

Notes:
1 – For applications requiring external 1/8” audio jacks, use Trenton part # 92-00677700. This board provides Line In, Line Out and Microphone
connections from the onboard audio codec to an I/O plate.

# Memory

## DDR4-2133 MEMORY

Trenton recommends unbuffered ECC PC4-17000 memory modules for use on the TKL8255. These unbuffered ECC registered (64-bit) DDR4 DIMMs must be PC4-17000 compliant. Unbuffered non-ECC DDR4 DIMMs are also supported on the TKL8255 SHB, but you cannot mix the two different memory types on the same board. The TKL8255 supports DDR4-1866 (PC4-14900) but optimal performance will not be achieved when these modules are utilized.

**NOTES:**

- To maximize memory interface speed, populate each memory channel with DDR4 DIMMs having the same interface speed. The SHB will support DIMMs with different speeds, but the memory channel interface will operate speed of the slowest DIMM.
- All memory modules must have gold contacts.
- All memory modules must have a 288-pin edge connector
- The SHB supports the following memory module memory latency timings:
  - 16-16-16 for 2133MHz DDR4 DIMMs
- Populate the memory sockets starting with memory channel A and begin by using the DIMM socket closest to the CPU first. Refer to the TKL8255 board layout drawing and populate the memory sockets using the population order illustrated in the chart below:

| Population order# | CPU1 |
|---|---|
| 1 | BK0A |
| 2 | BK1A |
| 3 | BK0B |
| 4 | BK1B |

#Using a balanced memory population approach ensures maximum memory interface performance. A "balanced approach" means using an even number of DIMMs on the TKL8255 SHB whenever possible.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board.

TKL8255 Product Detail