# MBC8240

## 8240-xxx

**No. 87-008240-000 Revision D**

## HARDWARE

## TECHNICAL REFERENCE

## Intel® Xeon® E3-1200 v3-series (Haswell)

## Quad Core

**PROCESSOR-BASED**

## Modular Blade Card

Also includes reference information for the:
MPI8241 – Mid-Plane Interface Board
BRC8244 – x16 PCIe Riser Card

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Modular blade card products from Trenton Systems are warranted against material and manufacturing defects for a period of 24 months from the date the product is shipped from Trenton's manufacturing/assembly facilities. Buyer agrees that if this product proves defective Trenton Systems, Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Systems' discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Systems, Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Systems, Inc. Trenton Systems, Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

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## RETURN POLICY

A Return Material Authorization (RMA) number, obtained from Trenton Systems prior to return, must accompany products returned for repair. The customer must prepay freight on all returned items, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Gainesville, GA facility:

Trenton Systems, Inc.
2350 Centennial Drive
Gainesville, GA 30504
Attn: Repair Department

Contact Trenton Systems for our complete service and repair policy.

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### HANDLING PRECAUTIONS

**WARNING:** This product has components that may be damaged by electrostatic discharge.

To protect your processor card (CARD) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the CARD in its static-shielded bag until you are ready to perform your installation.
- Handle the CARD by its edges.
- Do not touch the I/O connector pins.
- Do not apply pressure or attach labels to the CARD.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

### RECOMMENDED BOARD HANDLING PRECAUTIONS

This CARD has components on both sides of the PCB. Some of these components are extremely small and subject to damage if the board is not handled properly. It is important for you to observe the following precautions when handling or storing the board to prevent components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

# *Before You Begin*

### INTRODUCTION

It is important to be aware of the system considerations listed below before installing your MBC8240 (8240-xxx) CARD. Overall system performance may be affected by incorrect usage of these features.

### DDR3-1600 MEMORY

Trenton recommends unbuffered ECC PC3-12800 or PC3-10600 DDR3 memory modules for use on the MBC8240. These unbuffered ECC registered (64-bit) DDR3 DIMMs must be PC3-12800 or PC3-10600 compliant. Unbuffered non-ECC DDR3 DIMMs are also supported on the MBC8240 CARD, but you cannot mix the two different memory types on the same board.

**NOTES:**

- To maximize memory interface speed, populate each memory channel with DDR3 DIMMs having the same interface speed. The CARD will support DIMMs with different speeds, but the memory channel interface will operate speed of the slowest DIMM.
- All memory modules must have gold contacts.
- The CARD supports the following memory module memory latency timings:
  - 9-9-9 for 1333MHz DDR3 DIMMs
  - 11-11-11 for 1600MHz DDR3 DIMMs
- Populate the memory sockets starting with memory channel A and begin by using the DIMM socket closest to the CPU first. Refer to the MBC8240 board layout drawing and populate the memory sockets using the population order illustrated in the chart below:

| Population order[#] | CPU1 |
|---|---|
| 1 | BK0A |
| 2 | BK1A |
| 3 | BK0B |
| 4 | BK1B |

[#]Using a balanced memory population approach ensures maximum memory interface performance. A "balanced approach" means using an equal number of DIMMs on the MBC8240 CARD whenever possible.

The memory DIMMs on the CARD connect directly to the CPU and at least one memory module must be installed on the board.

### INTEL® AMT 9.0

Intel® AMT 9.0 is supported on the MBC8240 and includes useful features for managing clients remotely. Windows .Net Framework 3.5 or higher must be installed to avoid AMT x.x "unknown device" errors. Serial port console redirect and IDE-R are not currently supported in AMT 9.0 on the MBC8240.

### BIOS

The MBC8240 features the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. *(Note: the CARD's current MBCES008 BIOS has the Hibernate and Sleep states disabled.)* Details of the Aptio TSE are provided in the separate *MBC814 BIOS Technical Reference* manual.

### OPERATING SYSTEMS

Trenton Systems has successfully tested the MBC8240 processor card with a wide variety of operating systems including Linux (Red Hat RHEL, Centos and SUSE), Windows® Win7 (32 or 64-bit), Windows® 2008 Sever 64, Windows® Win8.1 64, Windows® 2012 Server 64, and Oracle® Solaris 11. However, there are some operating systems that Intel® does not recommend for use with the board's Haswell processor and Lynx Point PCH architecture, notably, Windows® XP (32 or 64-bit), and Windows® 2003 Server.

### FOR MORE INFORMATION

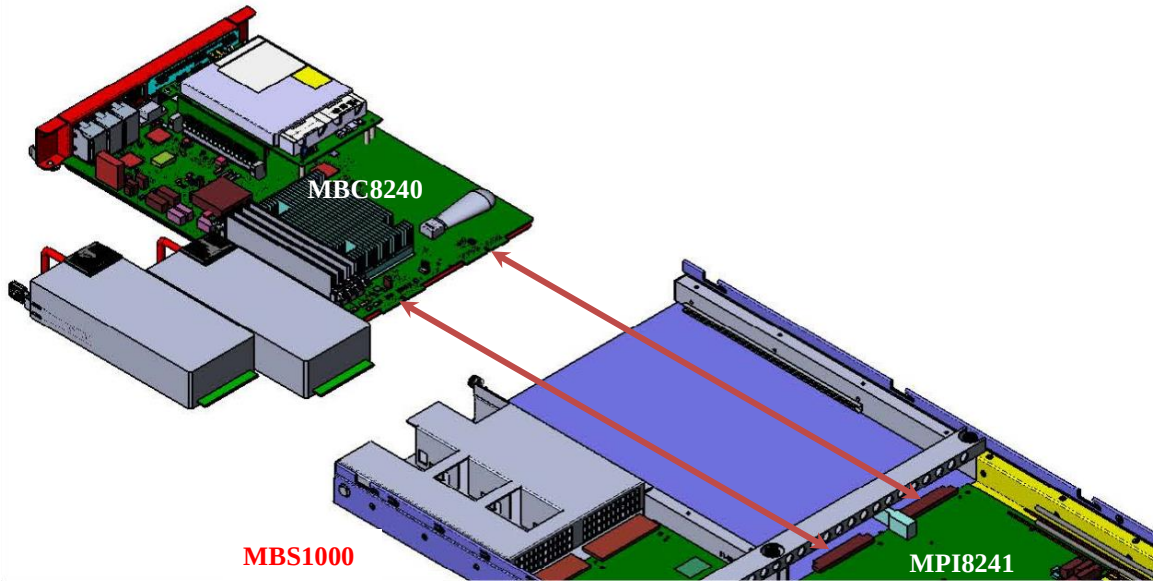
Refer to the appropriate sections *MBC8240Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the MBC8240 web page.

# *Chapter 1 Specifications*

**Introduction**

The MBC8240 is a modular blade card featuring the choice of a long-life/embedded, Intel® Xeon® E3-1200 v3 Series processor, formally known as Haswell. These processors utilize a 22nm micro-architecture, and have a DDR3-1600 integrated memory controller that supports two, dual-channel DDR3-1600 memory interfaces. The MBC8240 supports four DDR3 DIMM sockets. With 4GB, DDR3 DIMMs the total system memory capacity for a MBC8240 is 16GB and doubles to 32GB using 8GB DDR3 DIMMs.

The MBC8240 is designed to slide into a Trenton Systems' modular blade system chassis such as the 1U MBS1000. The MBC8240 used with the MBS1000 chassis is housed in a metal slide tray, and the full assembly slides into the rear card slot of the chassis. A mid-plane interface board (MPI8241) inside the MBS1000 engages with the two edge connectors at the rear of the MBC8240 as illustrated in the figure below.




**MBC8240 installation in a MBS1000 1U chassis**

System I/O features available on the MBC8240 include:

- A general purpose x16 PCI Express 3.0 mechanical expansion slot designed for use with the Trenton Systems BRC8244 PCIe riser card
- Six Gigabit Ethernet interface ports
- One additional Ethernet port for remote system management
- Three SATA/600 ports that can support independent drives or RAID drive arrays
- A total of 12 USB 2.0 interfaces are supported
  - Eight general purpose USB interfaces with six (6) are accessible on the card's I/O plate
  - Two (2) are available on the front panel of the MBS1000 chassis.
  - One internal USB interface dedicated to a special purpose USB dongle
- An RS232 high-speed serial interface port
- One VGA video port
- Integrated TPM 1.2 for Trusted Computing implementations
- Full Intelligent Platform Management Interface via Trenton Smart System Management implementation

**Processor Options**

The listing below summarizes the targeted embedded processors supported on the MBC8240 board.

| Model # | Model Name | Speed | Intel CPU Number |
|---|---|---|---|
| **Intel Xeon Processor (Haswell - WS) - Quad Core, 8MB cache, H-T, VT, TXT, ECC*:** | | | |
| 8240-002 | MBC/2.3HR8 | 2.3GHz | E3-1268L v3 |

* H-T = Intel Hyper-Threading, VT = Intel Virtualization Technology, TXT = Intel Trusted Execution Technology, ECC Memory Support

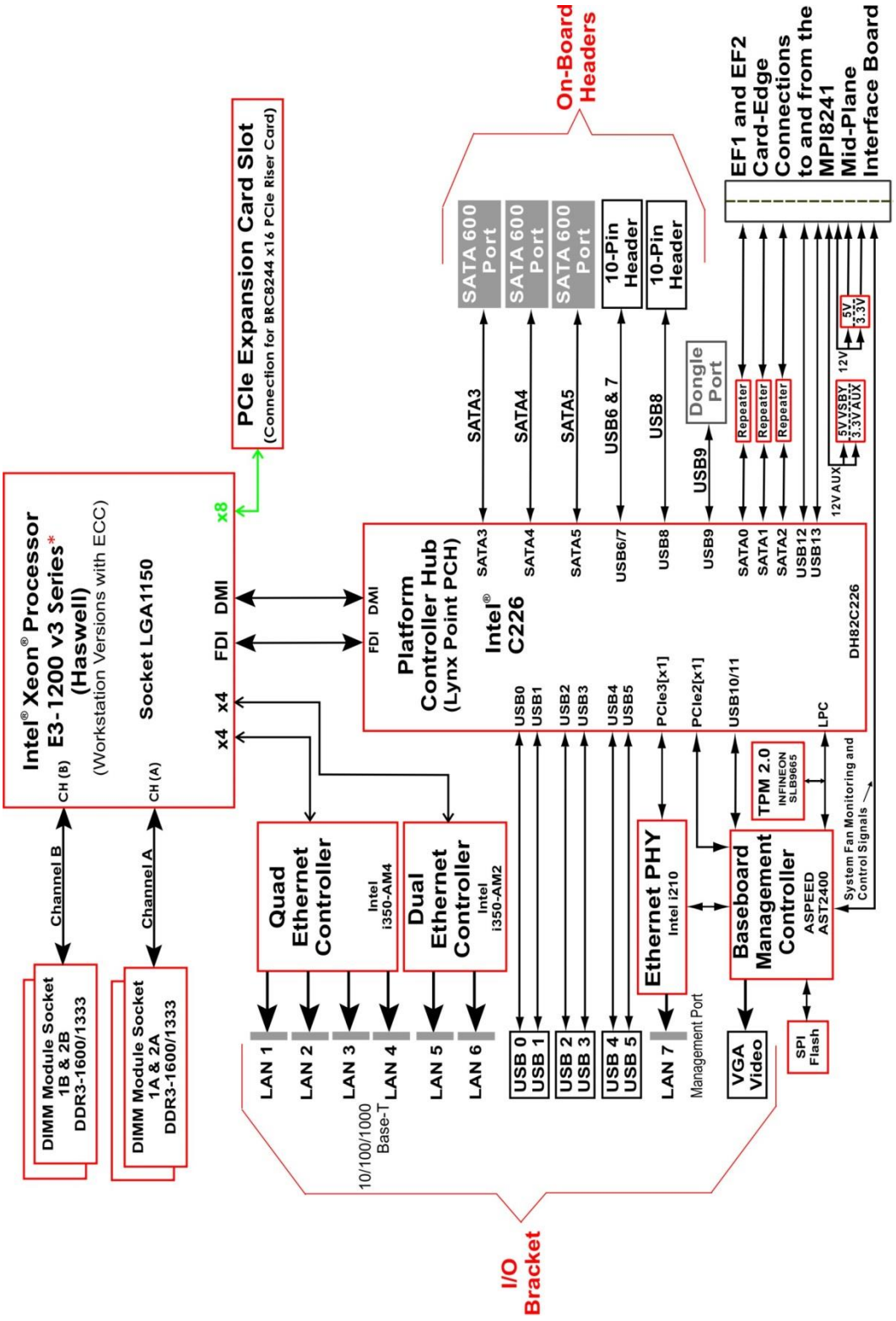
| | | | |
|---|---|---|---|
| **Intel Xeon Processor (Haswell - WS) - Quad Core, 8MB cache, VT, TXT, ECC:** | | | |
| 8240-013 | MBC/3.2H8 | 3.2GHz | E3-1225 v3 |

Additional embedded and non-embedded processor options are available for use on the MBC8240 processor card.

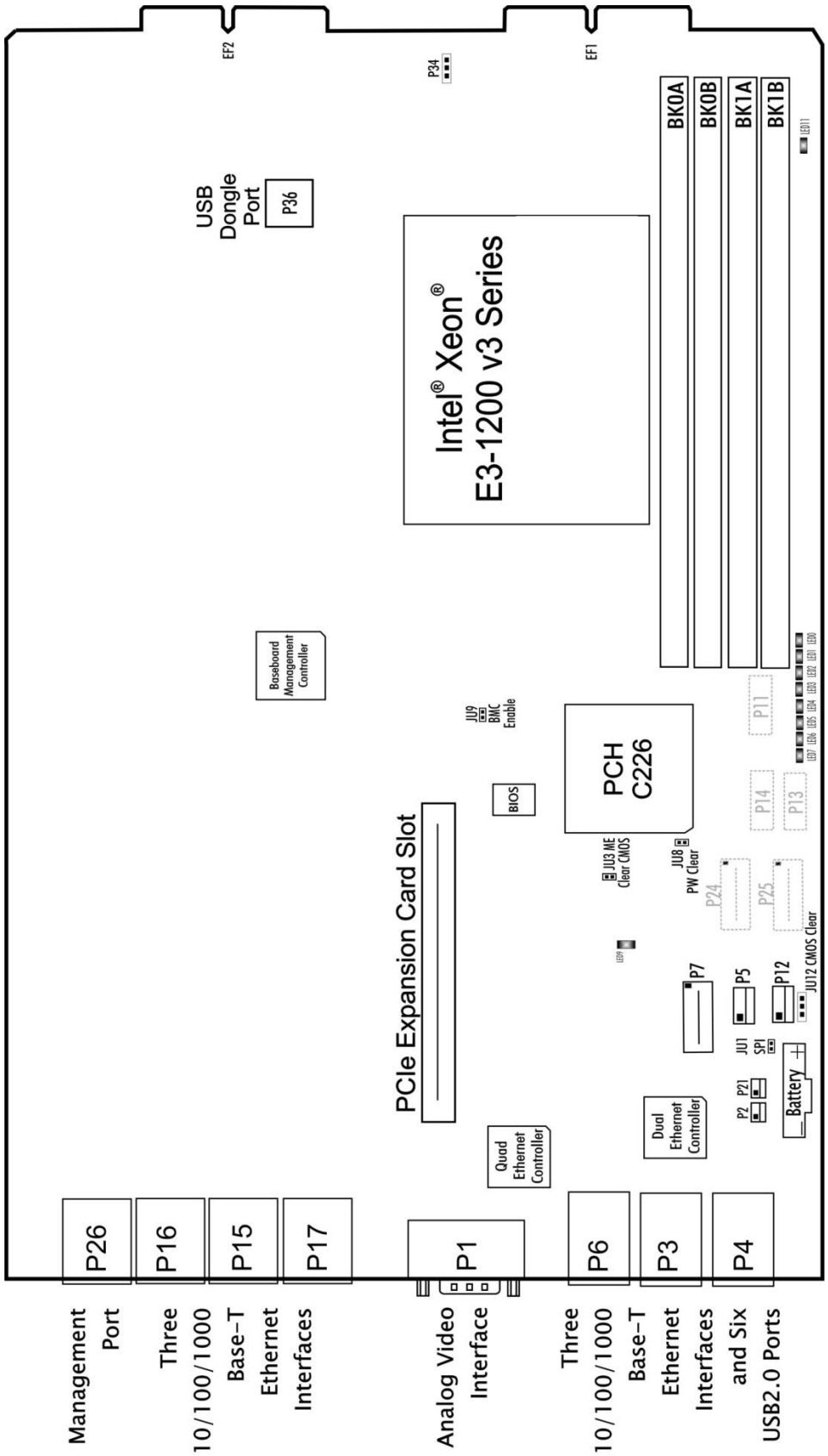
**Features**

- Intel® Xeon® E3-1200 v3 Series Processors (Haswell- WS)
- Intel® C226 Platform Controller Hub (Patsburg)
- Direct x8 PCI Express® 3.0 link from the processor to the board's x16 PCIe riser card slot
- A modular blade card format compatible with the MBS1000 1U rackmount chassis
- Direct DDR3-1600 Memory Interfaces into the Haswell Processor
- Four DDR3 DIMM sockets capable of supporting up to 32GB of system memory with 8GB DDR3 DIMMs and 16GB maximum capacity with readily available 4GB DDR3 DIMMs
- Six, general purpose 10/100/1000Base-T Ethernet interfaces available on the card's I/O plate
- One, 10/100/1000Base-T Ethernet interface dedicated to system management is also available on the card's I/O plate
- Three Serial ATA/600 ports support independent SATA storage devices and RAID 0, 1, 5 or 10 implementations *(Routed, but connectors are not populated, reserved for future usage)*
- Twelve Universal Serial Bus (USB 2.0) interfaces *(On-board connectors not populated, reserved for future usage)*
- Analog video port
- Metal carrier assembly for easy integration into a Trenton Systems' MBS1000 1U rackmount chassis
- Full PC compatibility
- Revision controlled Aptio 4.x BIOS for American Megatrends, Inc. (AMI) resides in the card's SPI flash device to simplify field upgrades and BIOS customization
    - See the ***BIOS Setup Manual*** for MBC8240 Processor card for more information

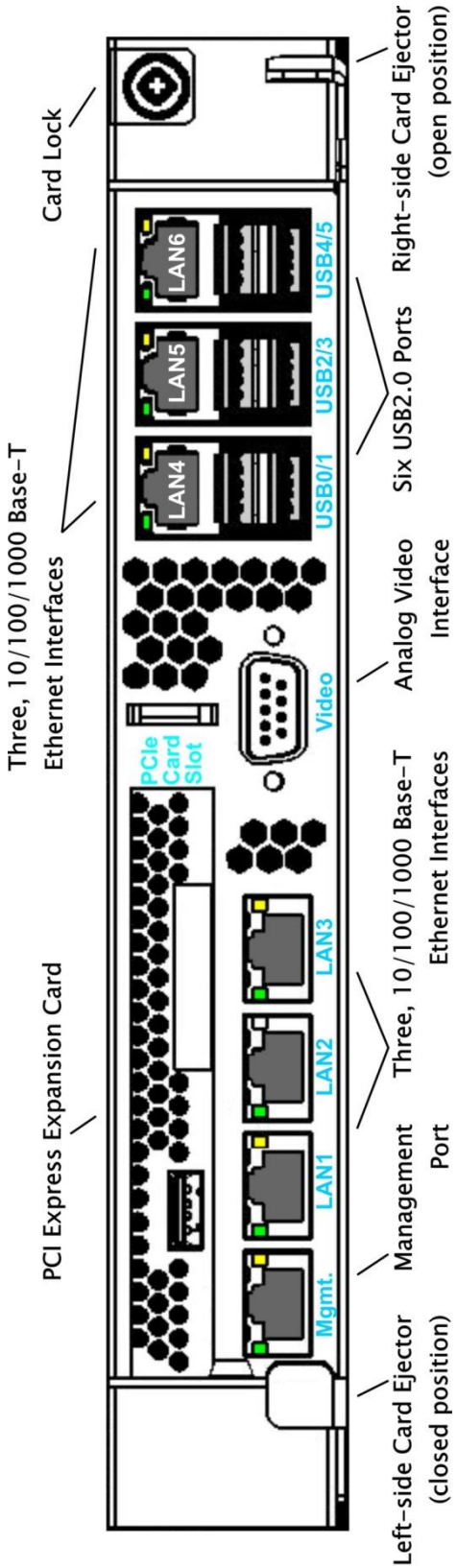
**MBC8240 (8240-xxx) – Single-Processor Modular Blade Card Block Diagram**



**MBC8240 (8240-xxx) – Single-Processor Modular Blade Card Layout Diagram**



**MBC8240 (8240-xxx) – Single-Processor Modular Blade Card I/O Bracket Layout**



**Processor**

- Intel® Xeon® E3-1200 v3 Series Processor – Long-life 22nm/Haswell Workstation processor
- Processor plugs into an LGA1150 socket

**Supported Intel® Processor Technologies**

The Intel® technologies supported on the MBC8240 processor card include:

- **Intel® Advanced Management Technology 9.0 (Intel® AMT)** – Provides the ability to monitor, maintain, update, upgrade, and repair a system remotely using one of the CARD's available Ethernet interfaces. Intel AMT is part of the processor's Intel Management Engine and the specific processor option selected for the use on the board must support Intel vPro technology in order to take full advantage of Intel AMT 9.0.

- **Intel® vPro** – Intel vPro is a combination of processor technologies, silicon hardware enhancements and management features that enable technologies like Intel AMT 9.0 to function.

- **Intel® Hyper-Threading (Intel® HT)** – This processor technology allows simultaneous multithreading of CPU tasks to enable parallel system operations. An operating system that is hyper-threading aware can address each core as a logical processor in order to spread out execution tasks to improve application software efficiency and overall system speed.

- **Intel Virtualization Technology (Intel® VT-x)** - Enabled in the CARD's BIOS, this technology enables multiple operating systems to run in specific Sandy Bridge processor cores thereby creating virtual machines (VMs) on a single CARD.

- **Intel Virtualization Technology for Directed I/O (Intel® VT-d)** – This is a sub-set of Intel VT-x and enables I/O device assignments to specific processor cores or VMs. Intel VT-d also supports DMA remapping, interrupt remapping and software DMA and interrupt status reporting. Intel VT-d is an optional extension to the Intel VT-x technology.

- **Intel® VT-x with Extended Page Tables (EPT)** –This feature is enabled in the Haswell micro-architecture to supports the processor's "real mode" or unrestricted guest feature.

- **Intel Trusted Execution Technology (Intel® TXT)** – This processor feature works in conjunction with the CARD's on-board Trusted Platform Module or TPM to allow the system designer to create multiple and separated execution environments or partitions with multiple levels of protection and security. The TPM provides for a way to generate and store an encrypted access key for authenticated access to sensitive applications and data. This private key never leaves the TPM, is generally available only to authorized system administrators, and enables remote assurance of a system's security state.

- **Intel Turbo Boost Technology 2.0** – The higher performance Haswell processors may run above the processors stated clock speed via a new dynamic processor speed control technology called Intel Turbo Boost 2.0. The processor enters the boost mode when the operating system requests the highest possible performance state as defined by the Advanced Configuration and Power Interface or ACPI.

- **Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI)** – Seven new instructions available in the Haswell micro-architecture makes pervasive encryption in an IT environment possible while enabling implementation that is faster and more affordable by providing advanced data protection and greater hardware platform security.

The following chart defines which Intel technology is supported on which particular embedded Haswell processor featured on the MBC8240 processor card.

| Intel Technology | Intel Xeon E3-1225 v3 | Intel Xeon E3-1268L v3 |
|---|---|---|
| Intel AMT 9.0 | Yes | Yes |
| Intel vPro | Yes | Yes |
| Intel HT | No | Yes |
| Intel Turbo Boost 2.0 | Yes | Yes |
| Intel VT-x | Yes | Yes |
| Intel VT-d | Yes | Yes |
| Intel VT-x with EPT | Yes | Yes |
| Intel TXT | Yes | Yes |
| Intel Turbo Boost 2.0 | Yes | Yes |
| Intel AES-NI | Yes | Yes |

**Serial Interconnect Interface**
PCI Express® 3.0, 2.0, and 1.1 compatible

**Data Path**
DDR3-1600 Memory - 64-bit (per channel)

**Serial Interconnect Speeds**
PCI Express 3.0 – 8.0GHz per lane
PCI Express 2.0 – 5.0GHz per lane
PCI Express 1.1 - 2.5GHz per lane

**Platform Controller Hub (PCH)**
- Intel® C226 Platform Controller Hub (Lynx Point)

**Intel® Direct Media Interface (DMI)**
The Haswell processors support the latest interface version called DMI. DMI supports communications between the board's processor and Intel® C226 PCH up to 20Gb/s each direction, full duplex and is transparent to software.

**Intel® Flexible Display Interface (FDI) Between CPU and PCH**
The FDI interconnect between the processor's display engine and the analog and digital video monitor interfaces connects to the Intel® C226 PCH. The FDI channel features differential signaling supporting 2.7Gb/s video data transfers for both single and dual monitor applications.

**Memory Interface**
The MBC8240 features two memory channels of unbuffered DDR3 with two DIMMs per channel. These DDR3-1600 memory interface channels support up to four, unbuffered, ECC PC3-12800 standard memory DIMMs. Non-ECC DDR3 DIMMs are also supported, but the two memory types cannot be used together on the CARD. The peak memory interface transfer rate per channel is 1600MT/s when using PC3-12800 DIMMs.

**DMA Channels**
The CARD is fully PC compatible with seven DMA channels, each supporting type F transfers.

**Interrupts**
The CARD is fully PC compatible with interrupt steering for PCI plug and play compatibility.

**BIOS (Flash)**
The MBC8240 board uses an Aptio® 4.x BIOS from American Megatrends Inc. (AMI). The BIOS features built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals and other system parameters. The BIOS resides in a 32Mb Atmel® AT25DF321SU SPI Serial EEPROM (SPI Flash). The BIOS may be upgraded from a USB thumb drive storage device by pressing **<Ctrl> + <Home>** immediately after reset or power-up with the USB device installed in drive A:. Custom BIOSs are available.

**Cache Memory**
The processors include either a 4MB, 6MB or 8MB Intel® Smart Cache memory capacity that is equally shared between all of the processor cores on the die.

**DDR3-1600 Memory**
The CARD supports two DDR3-1600 memory interface channels that can support two DIMMs each. The four active DIMM sockets on the MBC8240 models can support up to 8GB DIMMs for a total possible DDR3 system memory capacity of 32GB. However, the most common DDR3 DIMM memory capacities are 1GB, 2GB and 4GB. The system memory capacity limit when using 4GB DIMMS is 16GB. The peak memory interface transfer rate per channel is 1600MT/s when using PC3-12800 (i.e. DDR3-1600) DIMMs.

The System BIOS automatically detects memory type, size and speed. Trenton recommends unbuffered ECC PC3-12800 or PC3-10600 DDR3 memory modules for use on the MBC8240. These unbuffered ECC registered (64-bit) DDR3 DIMMs must be PC3-12800 or PC3-10600 compliant. Unbuffered non-ECC DDR3 DIMMs are also supported on the MBC8240 CARD, but you cannot mix the two different memory types on the same board.

**NOTES:**

- To maximize memory interface speed, populate each memory channel with DDR3 DIMMs having the same interface speed. The CARD will support DIMMs with different speeds, but the memory channel interface will operate speed of the slowest DIMM.
- All memory modules must have gold contacts.
- All memory modules must have a 240-pin edge connector
- The CARD supports the following memory module memory latency timings:
  - 9-9-9 for 1333MHz DDR3 DIMMs
  - 11-11-11 for 1600MHz DDR3 DIMMs
- Populate the memory sockets starting with memory channel A and begin by using the DIMM socket closest to the CPU first. Refer to the MBC8240 board layout drawing and populate the memory sockets using the population order illustrated in the chart below:

| Population order[#] | CPU1 |
|---|---|
| 1 | BK0A |
| 2 | BK1A |
| 3 | BK0B |
| 4 | BK1B |

[#]Using a balanced memory population approach ensures maximum memory interface performance. A "balance approach" means using an equal number of DIMMs on the MBC8240 CARD whenever possible.

The memory DIMMs on the CARD connect directly to the CPU and at least one memory module must be installed on the board. The MBC8240 CARD versions feature one processor; however, memory slots BK10, BK11 and BK12 are installed on the CARD but are not active in this single-processor board version.

**Universal Serial Bus (USB)**
The CARD supports a total of twelve USB interfaces. Two of the USB ports available for routing to the front panel connectors on located on the MBS1000 system. Six USB ports are found on the rear I/O bracket of the MBC8240. The remaining interfaces are routed to the cards on-board header connectors for use by other devices and sub-systems within a chassis like the MBS1000. On-board header connectors are not currently populated, and are reserved for future use.

**Analog Video Interface**
The MBC8240's PCIe graphics and remote management processor supports 2D video resolutions of 1920 x 1200 via the VGA port on the card's I/O bracket.

**PCI Express Card Interface**
A native x8 PCI Express® 3.0 link from the MBC8240's processor is routed to the card's x16 PCIe mechanical card slot. A x16 PCIe riser card; such as the Trenton BRC8244, engages with the PCIe card slot to enable electrical and mechanical support for an industry standard PCIe plug-in card installed in a 1U rackmount server such as the Trenton Systems MBS1000. This PCIe card slot link can operate as either a PCI Express 3.0, 2.0, or 1.1 link based on the option card connected to the riser card. This PCIe expansion slot fully supports PCI Express automatic link negotiation to enable card slot support for a x16, x8, x4 or x1 PCIe plug-in card.

**Serial ATA (SATA) Ports**
The three Serial ATA (SATA) ports on the card are driven with a built-in SATA controller from the Intel® C226 Platform Controller Hub (PCH). All of the card's SATA interfaces comply with the SATA 1.0, SATA 2.0, and SATA 3.0 specifications that define support for data transfer rates of 150MB/s, 300 MB/s, and 600MB/s respectively depending on the SATA device type connected.

The card's SATA controller may support up to three independent SATA storage devices such as hard disks and CD-RW devices. The SATA controller has two BIOS selectable modes of operation with a legacy (i.e. IDE) mode using I/O space, and an AHCI mode using memory space. Software that uses legacy mode will not have AHCI capabilities. SATA connectors are routed but not populated, and are reserved for future use.

**SATA RAID Operation (Windows O/S Setup)**
The Intel® C226 Platform Controller Hub (PCH) used on the card features Intel® Rapid Storage Technology (Intel® RST) and requires several unique drivers. A .zip file is available on the Trenton Systems website to help you configure the SATA ports as RAID drives connected to the MBC8240 while taking advantage of the PCH's drive array management.

The Microsoft Windows .NET framework 3.0 software framework includes libraries and other useful tools that allow the RST Rapid Storage Manager to install and function properly in reporting drive failure alerts correctly. Windows .NET Framework 3.0 or later may be required to support the latest revisions of the RST Rapid Storage Manager. Windows .NET Framework is already included with Windows 7 or Windows 2008 O/S installations but it does need to be enabled.

If you would like your system to immediately inform you of a failed drive in the RAID array then the "Hot Plug" setting on the Advanced/SATA MBC8240 BIOS screen needs to be ENABLED for each drive in the array. If this BIOS setting is DISABLED a drive failure notification alert may take several minutes or even longer if there is no hard drive activity on the RAID array.

**Ethernet Interfaces**
The MBC8240 supports seven Ethernet interfaces. All seven interfaces are located on the card's I/O bracket. Six of the interfaces are designed for general-purpose network connections, and are implemented using Intel® i350-AM4 Quad, and Intel® i350-AM2 Dual Gigabit Ethernet Controllers.

The seventh Ethernet interface comes from the card's PCIe graphics and remote management processor. This Ethernet interface is dedicated to the remote system management functions, referred to as Trenton Smart System Management, supported by the card's MPI implementation. All seven Ethernet interfaces

**Ethernet Interfaces (continued)**
support Gigabit, 100Base-T and 10Base-TX Fast Ethernet modes and are compliant with the IEEE 802.3 Specification.

**Trenton Smart System Management (SSM)**
The MBC8240 provides a full implementation of the industry-standard Intelligent Platform Management Interface (IPMI) via the onboard ASPEED AST2400 Baseband Management Controller (BMC). Access to these features is provided by a dedicated Ethernet LAN Port (Port 0) which ensures system security by physically isolating these features from the remaining Ethernet interfaces. SSM harnesses the Intelligent Platform Management Bus (IPMB), IPMI Platform Management Field Replaceable Unit (FRU) Information Storage Definition and Intelligent Chassis Management Bus (ICMB) to provide remote management and system health monitoring. Prominent features of the SSM implementation include:
• Fan speed monitoring
• Fan condition & status
• Alarm monitoring
• FRU management
• Voltage monitoring
• SBC present
• Remote messaging (i.e. call home)
• Poll for processor & memory health

Trenton Smart System Management allows for simplified management of computing deployments and helps ensure system health from anywhere in the world with a compatible Internet connection.

**Watchdog Timer (WDT)**
The MBC8240 provides a programmable watchdog timer with programmable timeout periods of 100 msec to 3 minutes via board component U11. When enabled the WDT (i.e. U11) will generate a system reset. WDT control is supplied via the General Purpose IO pins from the Intel® C226 Platform Controller Hub (PCH). The PCH's GPIO_LVL2 register controls the state of each GPIO signal. This 32-bit register is located within GPIO IO spaces. The GPIO_BASE IO address is determined by the values programmed into the PCH's LPC Bridge PCI configuration at offset 48-4B(h).

*GPIO Bit Definitions:*

Watchdog Timer Enable (WDT_EN#)
Watchdog timer enable\disable functionality is controlled by GPIO32. Clearing bit 0 of the GP_LVL register enables the WDT. The GP_LVL2 register is located at IO address GPIO_BASE + offset 38(h). The power-on default for this bit is a "1" which disables WDT functionality. Setting this bit to a "0" enables the WDT at the pre-selected interval.

Watchdog Select 0 (WDT_S0)
The state of this bit in conjunction with Watchdog Select 0 will select the WDT time out period. This function is controlled by GPIO33 and the state of this bit is determined by bit 1 of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST, the inverted state of this bit is reflected on Port80, LED0. If this bit is set to a "1" the LED is off, if set to a "0" the LED is on. The state of the GPIO pin is inverted at the Select 0 input of U11. See the Watchdog Timeout Period Selection table below for WDT interval selection information.

Watchdog Select 1 (WDT_S1)
The state of this bit in conjunction with Watchdog Select 1 will select the WDT time out period. This function is controlled by GPIO34 and the state of this bit is determined by bit three of the GP_LVL2 register at IO address GPIO_BASE + offset 38(h). After POST, the inverted state of this bit is reflected on Port80, LED1. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on. The state of the GPIO pin is inverted at the Select 0 input of U11. See the Watchdog Timeout Period Selection table below for WDT interval selection information.

**Watchdog Timer (WDT) (continued)**

Watchdog_ Input (WDT_IN)

When the WDT is enabled this bit must be toggled (0 -> 1 or 1->0) within the selected watchdog timeout period, failure to do so will result in a system reset. This function is supported by the GPIO71 bit and its state is controlled by bit 23 of the GP_LVL3 register which is at IO address GPIO_BASE + offset 48(h). The inverted state of this bit is reflected on Port80, LED7. If this bit is set to a "1" the LED in off, if set to a "0" the LED is on.

*Watchdog Timeout Period Selections:*

| WDT_EN# (GPIO32) | WD_S1 (GPIO34) | WD_S0 (GPIO33) | Watchdog Timeout Period |
|---|---|---|---|
| 1 | X | X | Disabled |
| 0 | 1 | 1 | 100msec |
| 0 | 1 | 0 | 1 sec |
| 0 | 0 | 1 | 10 sec |
| 0 | 0 | 0 | 1 min |

The Watchdog Timer may require initialization prior to usage. GPIO 32, 33, 34 and 71 must be configured as outputs. While these GPIOs do default to outputs at power-on, care should be taken to insure they have not been altered prior to WDT usage. These GPIO are configured to outputs by clearing bits 0, 1 and 2 of the GP_IO_SEL2 register at GPIO_BASE + offset 34(h) to a "0", as well as clearing bit 7 of the GP_IO_SEL3 register at GPIO_BASE + offset 44(h) to a "0".

After initialization is completed (if required) the Watchdog timer period is selected by via the WDT_S1 and WDT_S0 bits. Once the timeout period has been programmed the WDT is "enabled" by clearing the WDT_EN# bit. To avoid the WDT from generating a system reset the WDT_IN bit must be toggled within the timeout period.

*Programming Example: Enable WDT with 10-second timeout period*

***Note:*** *When writing to any of the WDT controlling GPIO bit the remaining bits of the selected GP_LVL2 and GP_LVL3 registers should remain unchanged.*

| | |
|---|---|
| Write bit 0 of GP_LVL2 to 1 | pre-condition GPIO32 for WDT disable |
| Write bits 2,1 of GP_LVL2 to 0,1 | set Watchdog timeout period to 10 sec |
| Write bit 0 of GP_LVL2 to 0 | enable Watchdog timer |

At this point, the bit 7 of GP_LVL3 (GPIO71) must be toggled within a 10 sec period or the WDT will expire resulting in a system reset.

**Power Fail Detection**

A hardware reset is issued when any of the voltages being monitored drops below its specified nominal low voltage limit. The monitored voltages and their nominal low limits are listed below.

| Monitored Voltage | Nominal Low Limit | Voltage Source |
|---|---|---|
| +5V | 4.75 volts | System Power Supply |
| +3.3V | 2.97 volts | System Power Supply |
| Vcc_DDR(+1.5V) | 1.15 volts | On-Board Regulator |
| VCCIO_CPU(1.05V) | 0.70 volt | On-Board Regulator |
| +1.05V(Chipset) | 0.924 volt | On-Board Regulator |
| +1.05V(Chipset-ME) | 0.924 volt | On-Board Regulator |

**Battery**
A built-in lithium battery is provided for ten years of data retention for CMOS memory.

**CAUTION:** There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the battery manufacturer. Dispose of used batteries according to the battery manufacturer's instructions.

**Temperature/Environment**
**Operating Temperature:** 0º C. to 40º C. for all CPU options

**Air Flow Requirement:** 350LFM continuous airflow

**Storage Temperature:** - 40º C. to 70º C.

**Humidity:** 5% to 90% non-condensing

**Mechanical**
The standard cooling solution used on the MBC8240 enables support for an industry standard, up to ¾-length, PCI Express plug-in card when using a x16 PCIe riser card such as the Trenton BRC8244. The card's overall dimensions are 14.250" (36.195cm) L x 9.000" (22.860cm) W.

**MBC8240 Card Carrier**
The MBC8240's full-length card carrier ensures the fast and safe insertion and removal of the card from 1U rackmount servers like the Trenton Systems MBS1000. The carrier card and its alignment pins maintain proper alignment within the card guides of a 1U rackmount computer chassis. The carrier's rugged backer plate design maximizes system reliability by shielding the card's rear-mounted components from mechanical damage.

**Mean Time Between Failures (MTBF)**
808,825 Power-On Hours (POH) at 40° C per Bellcore

**Industry Certifications**
This card is designed to meet a variety of internationally recognized industry standards including UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN61000-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996 and EN61000-4-11:1994.

### Configuration Jumpers

The setup of the configuration jumpers on the card is described below. An asterisk (*) indicates the default value of each jumper.

**NOTE:** For the three-position JU12 jumper, "RIGHT" is toward the card's battery; "LEFT" is toward the processor.

**JU1 Override SPI Write Protect Policies** (two position jumper)

Install for one power-up cycle to enable the board to unprotect the board's SPI storage device.
Remove for normal operation. *

**CAUTION:** Installing this jumper is only done for special board operations. Contact Trenton Systems technical support ***before*** installing this jumper to prevent any unintended system operation.

**JU3 Clear Management Engine (ME) Operational Parameters** (two position jumper)
The board's management engine has its own CMOS Non-Volatile Memory (NVM) that stores operational parameters for Intel AMT 9.0 implementations.

Install for one power-up cycle to clear management engine CMOS settings.
Remove for normal operation. *

**JU8 Clear Password** (two position jumper)

Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

**JU9 BMC Enable** (two position jumper)

Installing this jumper may be done to take the BMC out of the system for troubleshooting purposes. Installing this jumper will remove remote management capability from the system, and also cause the system fans to run at full speed.
This jumper is removed in normal operation. *

**CAUTION:** Installing this jumper is only done for special board operations. Contact Trenton Systems technical support ***before*** installing this jumper to prevent any unintended system operation.

**JU12 CMOS Clear** (three position jumper)
Install on the LEFT to clear.
Install on the RIGHT to operate. *

**NOTE:** To clear the CMOS, power down the system and install the JU12 jumper on the LEFT. Wait for at least two seconds, move the jumper back to the RIGHT and turn the power on. Clearing CMOS on the MBC8240 will not result in a checksum error on the following boot. If you want to change a BIOS setting, you must press DEL or the F2 key during POST to enter BIOS setup after clearing CMOS.

**Status LEDs**

**Ethernet LEDs and Connectors**

The I/O bracket houses the seven RJ-45 network connectors for general purpose Ethernet LAN network connections and the LAN interface for system management. Each LAN interface connector has two LEDs that indicate activity status and Ethernet connection speed. Listed below are the possible LED conditions and status indications for each LAN connector:

| LED/Connector | Description |
|---|---|
| Activity LED | Yellow LED that indicates network activity. This is the upper LED on the LAN connector (i.e., toward the upper memory sockets). |
| Off | Indicates there is no current network transmit or receive activity. |
| On (flashing) | Indicates network transmit or receive activity. |
| Speed LED | This multi-color LED identifies the connection speed of a card's Ethernet interface. These are the lower LEDs on the dual LAN connector |
| Green | Indicates a valid link at 1000-Mb/s or 1Gb/s. |
| Orange | Indicates a valid link at 100-Mb/s. |
| Off | Indicates a valid link at 10-Mb/s. |
| RJ-45 Network Connector | The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection |

**Status LEDs (continued)**

**Thermal Trip LED – LED9** (Labeled LED11 on Rev0 boards)
The thermal trip LED indicates when a processor reaches a shut-down state. The LED is located just above the SATA connector P28. LED9 indicates the processor shutdown status and thermal conditions as illustrated below:

| LED Status | Description |
|---|---|
| Off | Indicates the processor is operating within acceptable thermal levels |
| On (flashing) | Indicates the CPU is throttling down to a lower operating speed due to rising CPU temperature |
| On (solid) | Indicates the CPU has reached the thermal shutdown threshold limit. The CARD may or may not be operating, but a thermal shutdown may soon occur. |

**NOTE:** When a thermal shutdown occurs, the LED will stay on in systems using non- ATX/EPS power supplies. The CPU will cease functioning, but power will still be applied to the CARD. In systems with ATX/EPS power supplies, the LED will turn off when a thermal shutdown occurs because system power is removed via the ACPI soft control power signal S5. In this case, all CARD LEDs will turn off; however, stand-by power will still be present.

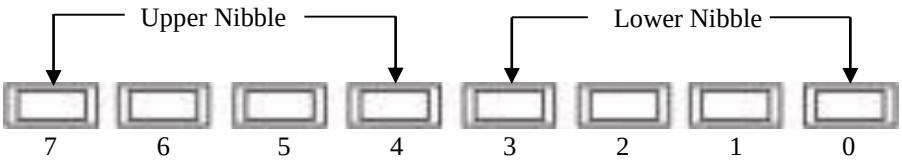
**VRM LED – LED11**
LED11 is a red LED located just above the left side of memory DIMM connector BK1B. If LED11 were to turn on and remain on, this would indicate that the voltage levels of the CARD's VRM circuits are not within the acceptable operating range. In all likelihood the CARD will fail to function if LED11 is on and the source of the voltage error could reside in the system power supply, the power supply wiring or on the board itself. Contact your system integrator or Trenton Tech Support for trouble shooting assistance.

**POST Code LEDs 0 - 7** (Labeled LEDs 1-8 on Rev0 boards)
As the POST, (Power On Self Test) routines are performed during boot-up; test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the CARD, just above the board's SATA connectors and slightly toward the right. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7). Refer to the board layout diagram for the exact location of the POST code LEDs.

These POST codes may be helpful as a diagnostic tool. After a normal POST sequence the LEDs are off (00h) indicating that the CARD's BIOS has passed control over to the operating system loader typically at interrupt INT19h. Specific test codes and their meaning along with the following chart are listed in Appendix A and can be used to interpret the LEDs into hexadecimal format during POST.

| Upper Nibble (UN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED7 | LED6 | LED5 | LED4 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |

| Lower Nibble (LN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED3 | LED2 | LED1 | LED0 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |




**MBC8240 POST Code LEDs**
(LED0 is located closest to the memory DIMM sockets)

**Thermal Trip LED – LED9**
LED9 is a red LED located between card component U2 and the P7 RS232 header connector. If LED9 were to turn on and remain on, this indicates that the card's VRM circuitry and/or processor has reached a temperature that exceeds maximum safe operational limits. The card is in a thermal shut down state when LED9 is on, and cannot operate until the fault condition is corrected. Contact your system integrator or Trenton Tech Support for trouble shooting assistance.

**VRM Fault LED – LED11**
LED11 is a red LED located just above the left side of memory DIMM connector BK1B. If LED11 were to turn on and remain on, this would indicate that the voltage levels of the card's VRM circuits are not within the acceptable operating range. In all likelihood the card will fail to function if LED11 is on. The source of the voltage error could reside in the system power supply, the power supply wiring or on the card itself. Contact your system integrator or Trenton Tech Support for trouble shooting assistance.

### System BIOS Setup Utility

The MBC8240 features the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. The TSE setup utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- Boot Setup
- Security Setup
- Chipset Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details of the Aptio TSE are provided in the separate *MBC8240BIOS Technical Reference* manual. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the MBC8240 web page.

## MBC8240 Connectors

**NOTE:** Pin 1 on the connectors is indicated by the square pad on the PCB.

**P1** - **Analog Video Interface Connector**
15 position socket connector, AMP 748390-5

| Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|
| 1 | Red | 6 | GND | 11 | NC |
| 2 | Green | 7 | GND | 12 | EEDI |
| 3 | Blue | 8 | GND | 13 | HSYNC |
| 4 | NC | 9 | +5 | 14 | VSYNC |
| 5 | GND | 10 | GND | 15 | EECS |

Note: Video connector supports standard DB15 analog video cables

**P2** - **Reset Connector**
2 pin single row header, Amp #640456-2

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GND | 2 | Reset In |

**P3, P4, P6** - **Dual Universal Serial Bus (USB) 2.0 Connectors** (Part of the three integrated Ethernet connectors)
Dual USB ports, WURTH #7497111611A
(+5V fused with self-resetting fuses)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB*n* | 5 | +5V-USB*n* |
| 2 | USB*n*- | 6 | USB*n*- |
| 3 | USB*n*+ | 7 | USB*n*+ |
| 4 | GND-USB*n* | 8 | GND-USB*n* |

Notes:
1 - The letter *n* indicates USB port number: 0, 1, 2, 4, or 5.
2 - P3 = USB2 and USB3, P4 = USB4 and USB5, P6 = USB0 and USB1

**P5** - **Speaker Port Connector**
4 pin single row header, Amp #640456-4

| Pin | Signal |
|---|---|
| 1 | Speaker Data |
| 2 | NC |
| 3 | GND |
| 4 | +5V |

**P3A, P4A, P6A** - **General Purpose 10/100/1000Base-T Ethernet Connectors - LAN4, LAN5, LAN6**
Integrated RJ-45 connector for P3A, P4A and P5A, WURTH #7497111611A
Note: Connector housings P3A, P4A and P6A also contain dual USB ports
Each individual RJ-45 connector is defined as follows:

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Signal GND | 9 | L*n*_MDI3+ |
| 2 | L*n*_MDI0n+ | 10 | L*n*_MDI3- |
| 3 | L*n*_MDI0- | 11 | L*n*_LINK# |
| 4 | L*n*_MDI1+ | 12 | L*n*_ACTV# |
| 5 | L*n*_MDI1- | 13 | NC |
| 6 | LAN*n*_TCT (VCC) | 14 | L*n*_LINK100 |
| 7 | L*n*_MDI2+ | 15 | L*n*_LINK1000# |
| 8 | L*n*_MDI2- | 16 | NC |

Notes:
1 - LAN ports support standard CAT5 Ethernet cables
2 - The letter *n* indicates Ethernet LAN port number: 4, 5, or 6
3 - P3A is LAN5, P4A is LAN6, P6A is LAN4

**Connectors** (Continued)

**P7** - **Serial Port Header Connector – RS232 Signal Connections**

10 pin dual row header, Amp #5103308-1

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Carrier Detect | 2 | Data Set Ready-I |
| 3 | Receive Data-I | 4 | Request to Send-O |
| 5 | Transmit Data-O | 6 | Clear to Send |
| 7 | Data Terminal Ready-O | 8 | Ring Indicator-I |
| 9 | GND | 10 | NC |

**P15, P16, P17,** - **General Purpose 10/100/1000Base-T Ethernet Connectors - LAN1, LAN2, LAN3**

Individual RJ-45 connector for P15, P16 and P17, PULSE # J0G-0009NL

Each individual RJ-45 connector is defined as follows:

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | LAN*n*_TCT3 | 11 | L*n*_MDI0n+ |
| 2 | L*n*_MDI2- | 12 | LAN*n*_TCT1 |
| 3 | L*n*_MDI2+ | 13 | L*n*_LINK# |
| 4 | L*n*_MDI1+ | 14 | L*n*_ACTV# |
| 5 | L*n*_MDI1- | 15 | NC |
| 6 | LAN*n*_TCT2 | 16 | L*n*_LINK100# |
| 7 | LAN*n*_TCT4 | 17 | L*n*_LINK1000# |
| 8 | L*n*_MDI3+ | 18 | Shield GND |
| 9 | L*n*_MDI3- | 19 | Shield GND |
| 10 | L*n*_MDI0- | | |

Notes:

1 - LAN ports support standard CAT5 Ethernet cables

2 - The letter *n* indicates Ethernet LAN port number: 1, 2, or 3

3 - P15 is LAN2, P16 is LAN1, P17 is LAN3

**P11, P13, P14** - **SATA Ports**

7 pin vertical locking connector, Molex #67800-8005

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | TX+ |
| 3 | TX- |
| 4 | GND |
| 5 | RX+ |
| 6 | RX- |
| 7 | GND |

Notes:

1 – P11 = SATA5, P13 = SATA4, P14 = SATA3

2 – SATA connectors support standard SATA II interface cables

3 – All SATA interfaces support SATA 3.0, SATA 2.0 and SATA 1.0 devices

4 – SATA 3.0 = 600MB/s data transfers, SATA 2.0 = 300MB/s data transfers and SATA 1.0 = 150MB/s data transfers

5 - On-board connectors not populated, reserved for future usage.

**P12** - **Hard Drive LED Connector**

4 pin single row header, Amp #640456-4

| Pin | Signal |
|---|---|
| 1 | LED+ |
| 2 | SATA_LED# |
| 3 | SATA_LED# |
| 4 | LED+ |

**Connectors** (Continued)

**P21** - **Power Good LED Header**

2 pin single row header, Amp #640456-2

| Pin | Signal |
|---|---|
| 1 | PWRGDLED# |
| 2 | +3.3V |

**P24, P25** - **Dual Universal Serial Bus (USB) 2.0 Headers**

*(On-board connectors not populated, reserved for future usage.)*

10 pin dual row header, Amp #1761610-3

(+5V fused with self-resetting fuses)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB*n* | 2 | +5V-USB*n* |
| 3 | USB*n*- | 4 | USB*n*- |
| 5 | USB*n*+ | 6 | USB*n*+ |
| 7 | GND-USB*n* | 8 | GND-USB*n* |
| 9 | NC | 10 | NC |

Notes:

1 - The letter *n* indicates USB port number: 6, 7, 8, or 9.

2 – P24 = USB6 and USB7, P25 = USB8 and USB9

**P26** - **Remote System Management 10/100/1000Base-T Ethernet Connector – LAN7**

Individual RJ-45 connector, PULSE # J0G-0009NL

RJ-45 remote system management connector is defined as follows:

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TCT3 | 11 | MDI0n+ |
| 2 | MDI2- | 12 | TCT1 |
| 3 | MDI2+ | 13 | +3.3V |
| 4 | MDI1+ | 14 | ACTV# |
| 5 | MDI1- | 15 | NC |
| 6 | TCT2 | 16 | LINK1000# |
| 7 | TCT4 | 17 | LINK100# |
| 8 | MDI3+ | 18 | Shield GND |
| 9 | MDI3- | 19 | Shield GND |
| 10 | MDI0- | | |

Notes:

1 - LAN port supports standard CAT5 Ethernet cables

2 - P26 is LAN7 and is dedicated to support remote system management functions

**P34** - **SMBus Clock Header**

3 pin single row header, Amp #640456-3

| Pin | Signal |
|---|---|
| 1 | VSMBDAT |
| 2 | VSMBCLK |
| 3 | GND |

**P36** - **USB PORT9 Dongle Header Connector**

USB9 dongle port, FOXCONN #UB1112C-4HK2-4F

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB9 | 4 | GND |
| 2 | USB9- | 5 | GND |
| 3 | USB9+ | 6 | GND |

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# *Chapter 2 PCI Express® Reference*

**Introduction**

PCI Express® is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the MBC8240 processor card and an industry standard, plug-in PCI Express option card.

Any PCI Express option card may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification.

The MBC8240 is designed for easy insertion in a 1U rackmount server chassis such as the Trenton Systems MBS1000. The 1U rackmount mechanics require the use of a PCI Express riser card in order to enable the MBC8240 to interface to an industry standard, ½-length or less, PCIe plug-in card. The BRC8244 riser card from Trenton Systems utilizes x16 PCIe connectors to accommodate a x1, x4, x8 or x16 PCI Express option card. PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector. The PCIe automatic link negotiation inherent in the interface protocol enabled cards like the MBC8240 to establish an interface link regardless of the option card's PCIe interface type.

**PCI Express Links**

There are several PCI Express links on the MBC8240. Most of these links are used for connecting card components together electrically. For instance, the card's dual and quad-channel Ethernet controllers are each driven with a x4 PCIe 2.0 link from the MBC8240's processor. A couple of x1 PCIe 2.0 links from the card's Platform Controller Hub (PCH) connect with the Ethernet PHY for the system management interface (LAN7) and the MBC8240's PCIe graphics and remote management processor. The card's PCI Express option card slot is a x16 mechanical slot driven by a native x8 PCIe 3.0 electrical link direct from the MBC8240's processor.

A PCI Express link is a collection of one or more PCIe lanes. A basic full-duplex link consists of two dedicated lanes for receiving data and two dedicated lanes for transmitting data. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, referred to as a x1, x4, x8 and x16 card slot when connecting a general purpose PCI Express plug-in card to a card slot on a backplane or a processor card. A x1 slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth for each version of PCI Express listed below ranges from 500MB/s up to 2GB/s (full-duplex).

The number and configuration of a processor card's PCI Express links is determined by specific component PCI Express specifications. In PCI Express Gen1.1 the bandwidths for the PCIe links are determined by the link width multiplied by 250MB/s and 500MB/s, as follows:

| Slot Size | Bandwidth | Full-Duplex Bandwidth |
|---|---|---|
| x1 | 250MB/s | 500MB/s |
| x4 | 1GB/s | 2GB/s |
| x8 | 2GB/s | 4GB/s |
| x16 | 4GB/s | 8GB/s |

**PCI Express Links** (continued)
In PCIe Gen2 the bandwidths for the PCIe links are doubled as compared to PCIe Gen1.1 as shown below:

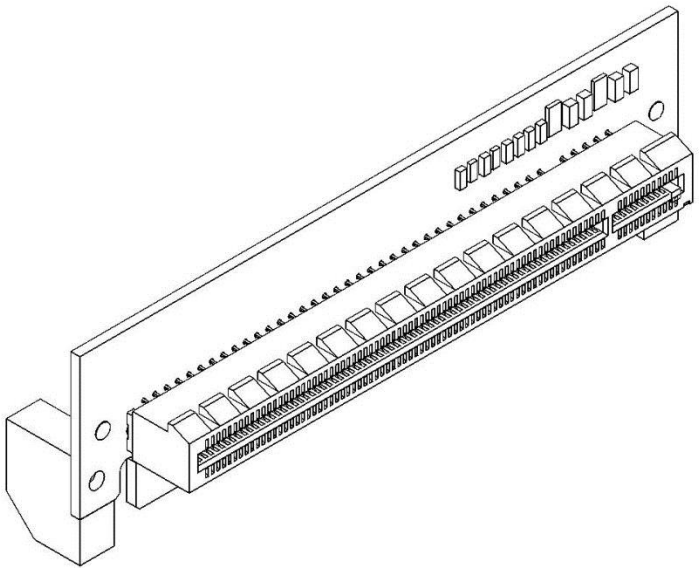
| Slot Size | Bandwidth | Full-Duplex Bandwidth |
|---|---|---|
| x1 | 500MB/s | 1GB/s |
| x4 | 2GB/s | 4GB/s |
| x8 | 4GB/s | 8GB/s |
| x16 | 8GB/s | 16GB/s |

Link protocol changes and speed increases double PCIe Gen3 bandwidths compared to PCIe Gen2 speeds:

| Slot Size | Bandwidth | Full-Duplex Bandwidth |
|---|---|---|
| x1 | 1GB/s | 2GB/s |
| x4 | 4GB/s | 8GB/s |
| x8 | 8GB/s | 16GB/s |
| x16 | 16GB/s | 32GB/s |

Scalability is a core feature of the PCI Express protocol. Some processors and PCHs allow a PCI Express link to be subdivided into additional links, e.g., a x8 link may be able to be divided into two x4 links. An option card with a higher number of lanes can be made to function in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) if the card slot is large enough mechanically. For example, a card with a x16 electrical interface can function in the x8 electrical slot of the MBC8240 because both the card and riser slot used mechanical x16 PCIe edge and slot connectors. Conversely, an option card with a lower number of lanes can be placed into a slot with a higher number of lanes (e.g., a x4 board into a x8 electrical slot). In these examples the x8 PCI Express link on the MBC8240 card slot auto-negotiates between the PCI Express devices to establish communication.

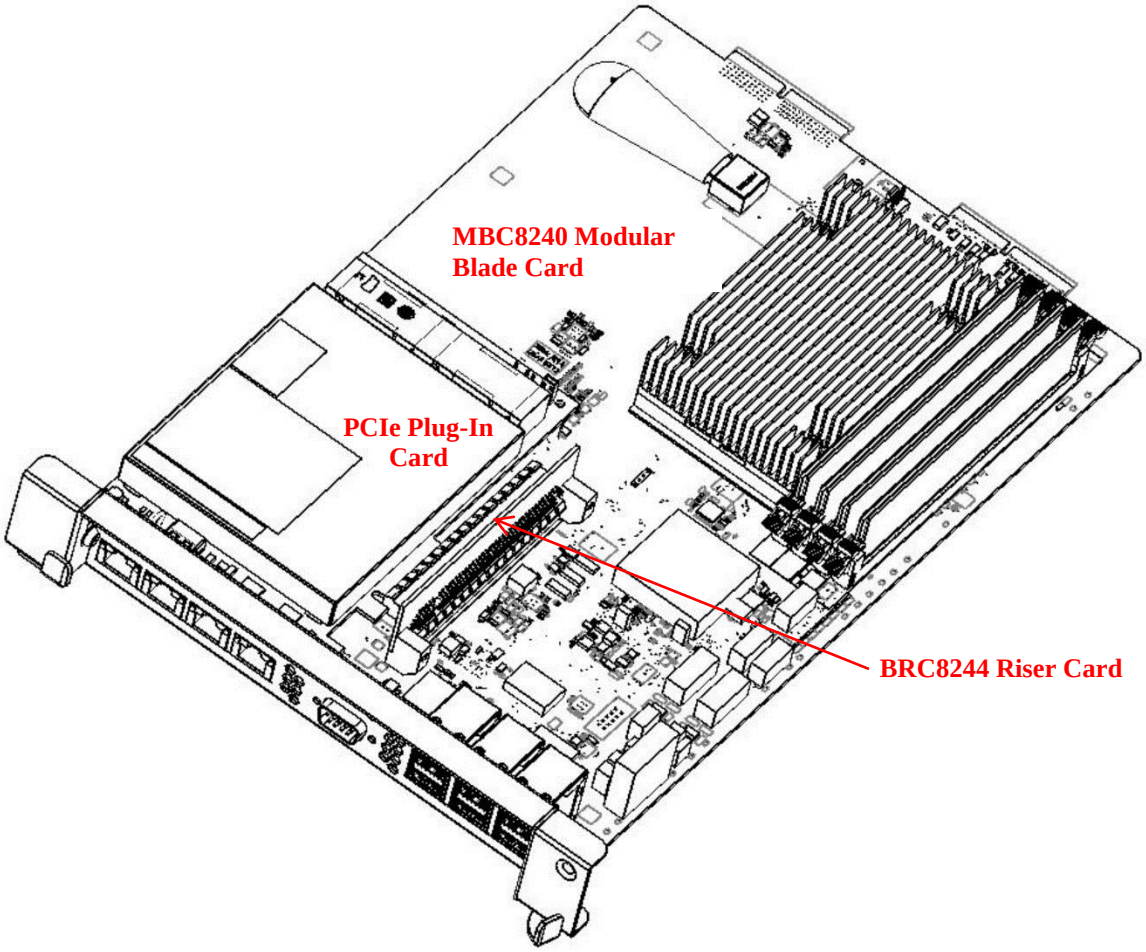
**Card Configuration**
The MBC8240 is a processor card designed to support an industry standard, plug-in PCI Express option card via a standard mechanical x16 PCIe riser card such as the Trenton BRC8244. Both the riser card and the MBC8240 use x16 PCIe mechanical edge connectors and/or card slots.



**BRC8244 x16 PCI Express Riser Card**

**Card Configuration (continued)**

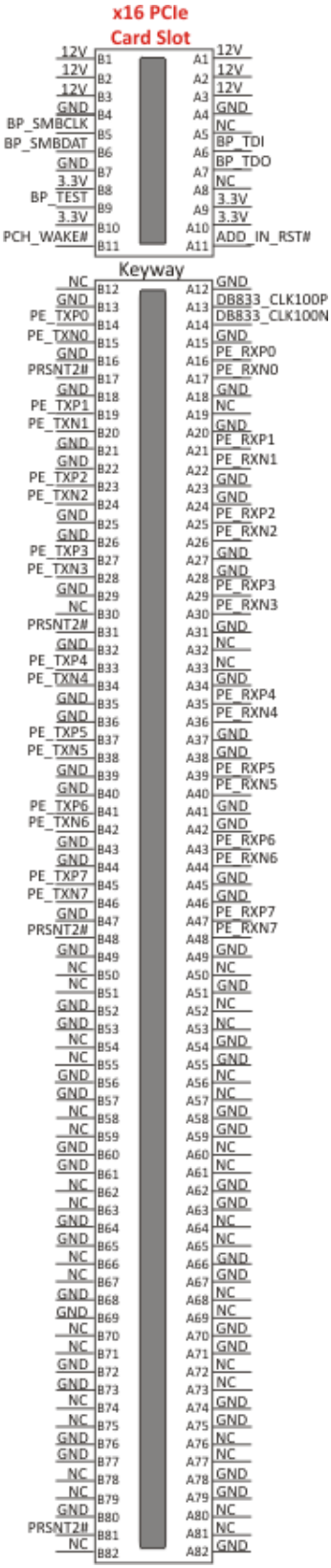
The MBC8240's x16 mechanical PCIe card slot is driven with x8 PCI Express 3.0 electrical link. Using the BRC8244 riser card as show in the illustration below will enable the system to support an industry standard, ½-length or less, PCIe plug-in card. The PCIe automatic link negotiation features supported by the MBC8240 processor, coupled with the x16 PCIe connectors on the BRC8244 riser card enables system support for a PCIe plug-in card with either a x1, x4, x8 or x16 PCI Express 1.1, 2.0, or 3.0 electrical interface.




**MBC8240 Modular Blade Card with the BRC8244 x16 PCI Express Riser Card Supporting a PCI Express Plug-In Card**

**PCI Express Edge Connector Pin Assignments**

Trenton's MBC8240 pin assignments for the PCI Express option card slot are listed in the figure below.



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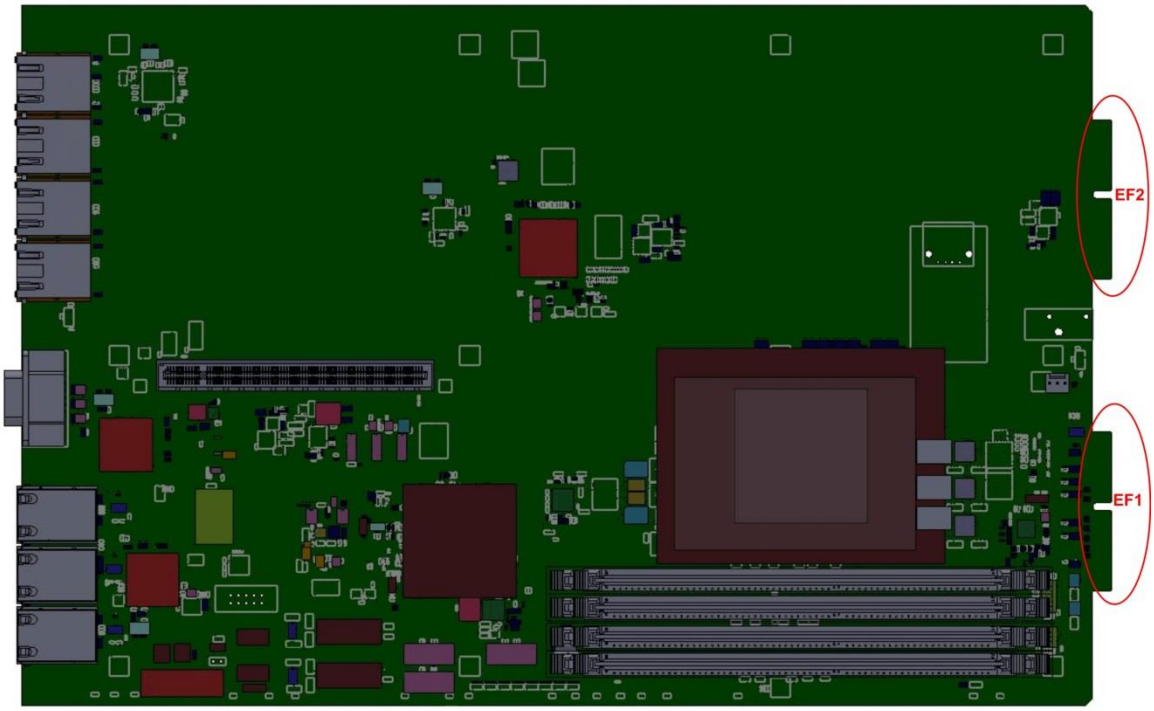
# *Chapter 3 MBC8240 System Connections*

**Introduction**

To improve 1U rackmount system MTTR (Mean Time To Repair), the MBC8240 modular blade card features two edge card connectors designed to engage with slot connectors P7 and P8 on a mid-plane interface board such as the Trenton MPI8241. This mechanical design approach allows easy field replacements and upgrades of the MBC8240 by enabling the card to easily slide into and out of a 1U rackmount chassis such as the Trenton MBS1000. The illustrations below define the locations and pin-outs of the MBC8240's two edge card connectors.



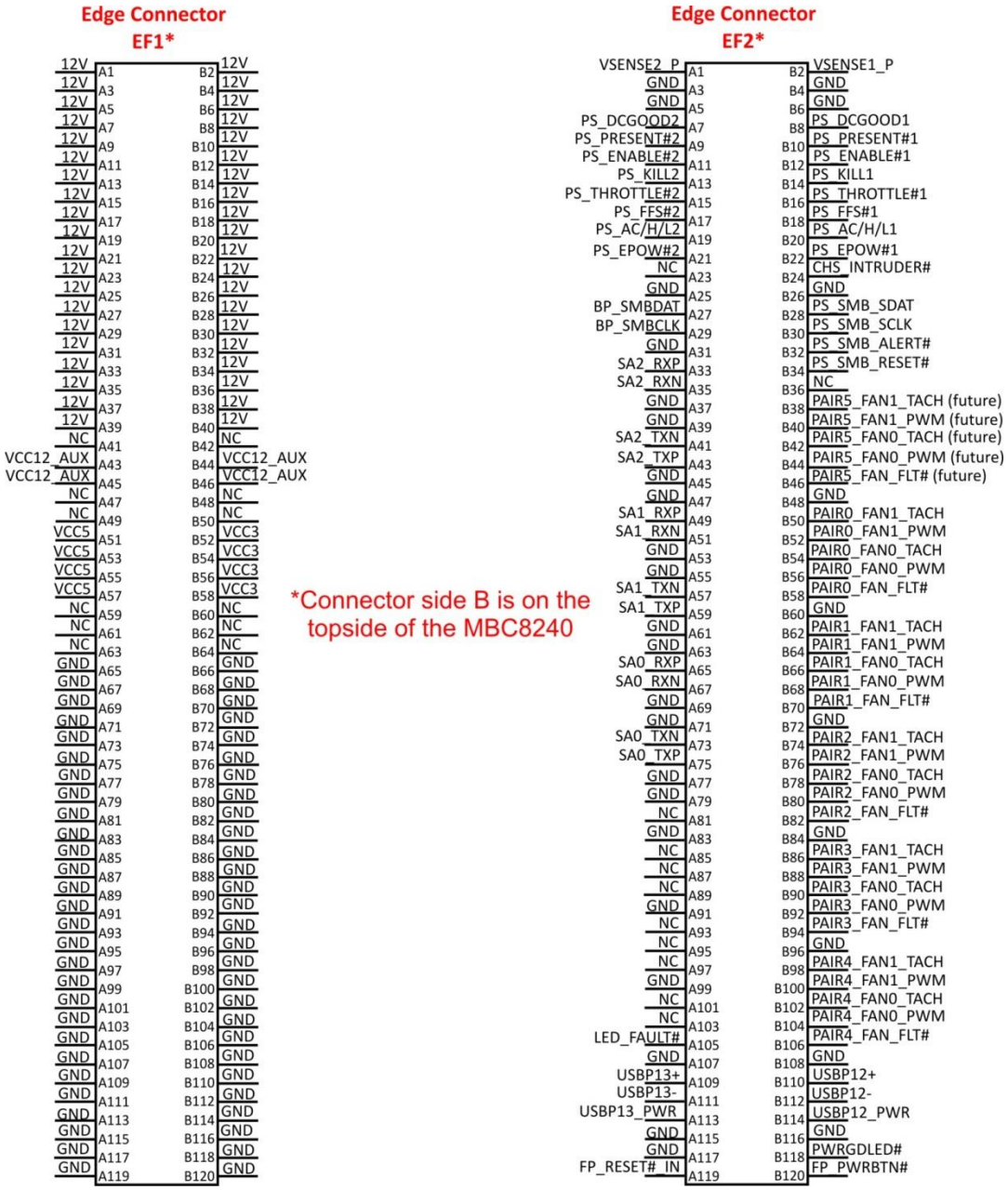

**MBC8240 Modular Blade Card with Edge Connectors EF1 and EF2 Highlighted**

Notes:

1. Side B of the EF1 and EF2 card edge fingers are located on the topside of the MBC8240 card.
2. When sliding the MBC8240 into a Trenton Systems MBS1000 ensure that the injector/ejector tabs on the cards' I/O bracket are in the open position.
3. Alignment guides in the MBS1000 chassis will ensure that the EF1 and EF2 edge connectors align properly with the mating socket connectors on the MPI8241 mid-plane interface board.
4. Slide the MBC8240 assembly into the MBS1000 until the card edge connectors fully engage with the mid-plane socket connectors.
5. Close the injector/ejector tabs to lock the MBC8240 assembly into the chassis.

**MBC8240 Edge Card Connector Signals (EF1 and EF2)**

The cart below provides a detailed listing of the signal routings on MBC8240 edge connector EF1 and EF2. Remember that side B of each edge connector is located on the topside of the MBC8240.




**MBC8240 Modular Blade Card with Edge Connectors EF1 and EF2 Signal Layout**

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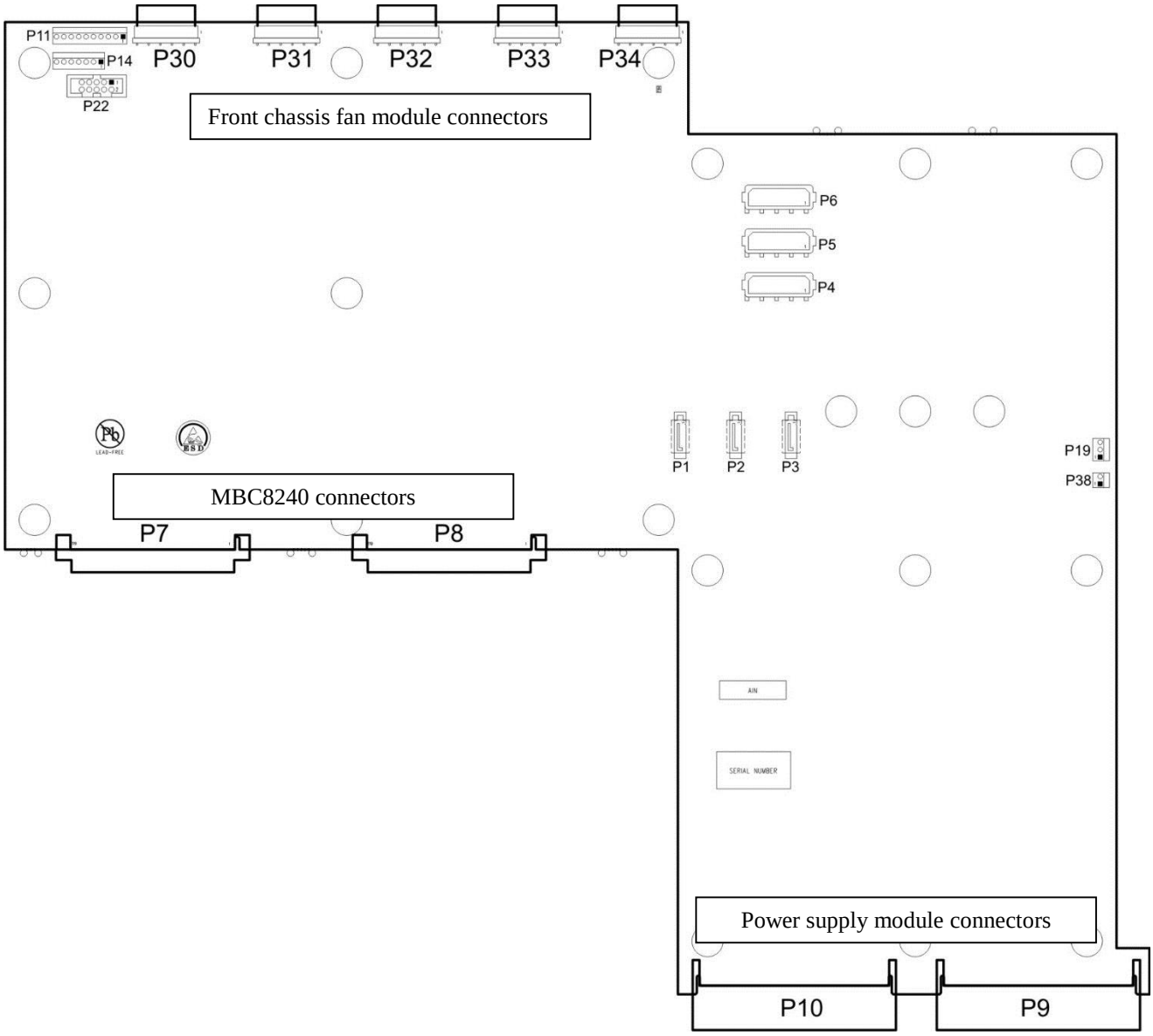
# *Chapter 4 MPI8241 Mid-Plane Interface Board Connections*

**Introduction**

The MPI8241 mid-plane interface board enables a 1U rackmount system such as the Trenton MBS1000 modular blade server, to support fast field replacements of various system sub-components. Specifically, the MPI8241enables easy access to the following MBS1000 field replaceable units or FRUs:

- MBC8240 Modular Blade Card
- Storage drives (2 per drive carrier maximum)
- Optical media drive (1)
- Power supply modules (2)
- Front system fan modules (5)
- OIB8247 operator interface board (future)




**MPI8241 Mid-Plane Interface Board**

### MPI8241 Mid-Plane Connectors

**NOTE:** Pin 1 on the connectors is indicated by the square pad on the PCB.

**P1, P2, P3** - **SATA Ports**

7 pin vertical locking connector, Molex #67800-8005

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | TX+ |
| 3 | TX- |
| 4 | GND |
| 5 | RX+ |
| 6 | RX- |
| 7 | GND |

Note: P1 = SATA0, P2 = SATA1, P3 = SATA2

**P4, P5 P6** - **Drive Power Connectors**

4 pin single row power header, Amp #1586627-1

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | 12V | 3 | GND |
| 2 | GND | 6 | 5V |

**P7** - **Mating Socket Connector for the EF2 MBC8240 Edge Card Connector**

120 position dual row connector, Samtec #HSEC8-160-01-S-D-EM2

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | 12V | 3 | 12V | 4 | 12V |
| 5 | 12V | 6 | 12V | 7 | 12V | 8 | 12V |
| 9 | 12V | 10 | 12V | 11 | 12V | 12 | 12V |
| 13 | 12V | 14 | 12V | 15 | 12V | 16 | 12V |
| 17 | 12V | 18 | 12V | 19 | 12V | 20 | 12V |
| 21 | 12V | 22 | 12V | 23 | 12V | 24 | 12V |
| 25 | 12V | 26 | 12V | 27 | 12V | 28 | 12V |
| 29 | 12V | 30 | 12V | 31 | 12V | 32 | 12V |
| 33 | 12V | 34 | 12V | 35 | 12V | 36 | 12V |
| 37 | 12V | 38 | 12V | 39 | 12V | 40 | 12V |
| 41 | NC | 42 | NC | 43 | 12V_AUX | 44 | 12V_AUX |
| 45 | 12V_AUX | 46 | 12V_AUX | 47 | NC | 48 | NC |
| 49 | NC | 50 | NC | 51 | 5V | 52 | 3.3V |
| 53 | 5V | 54 | 3.3V | 55 | 5V | 56 | 3.3V |
| 57 | 5V | 58 | 3.3V | 59 | NC | 60 | NC |
| 61 | NC | 62 | NC | 63 | NC | 64 | NC |
| 65 | GND | 66 | GND | 67 | GND | 68 | GND |
| 69 | GND | 70 | GND | 71 | GND | 72 | GND |
| 73 | GND | 74 | GND | 75 | GND | 76 | GND |
| 77 | GND | 78 | GND | 79 | GND | 80 | GND |
| 81 | GND | 82 | GND | 83 | GND | 84 | GND |
| 85 | GND | 86 | GND | 87 | GND | 88 | GND |
| 89 | GND | 90 | GND | 91 | GND | 92 | GND |
| 93 | GND | 94 | GND | 95 | GND | 96 | GND |
| 97 | GND | 98 | GND | 99 | GND | 100 | GND |
| 101 | GND | 102 | GND | 103 | GND | 104 | GND |
| 105 | GND | 106 | GND | 107 | GND | 108 | GND |
| 109 | GND | 110 | GND | 111 | GND | 112 | GND |
| 113 | GND | 114 | GND | 115 | GND | 116 | GND |
| 117 | GND | 118 | GND | 119 | GND | 120 | GND |

**Connectors** (continued)

**P8** - **Mating Socket Connector for the EF1 MBC8240 Edge Card Connector**
120 position dual row connector, Samtec #HSEC8-160-01-S-D-EM2

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | VSENSE2_P | 2 | VSENSE1_P | 3 | VSENSE2_N | 4 | VSENSE1_N |
| 5 | GND | 6 | GND | 7 | DCGOOD2 | 8 | DCGOOD1 |
| 9 | PRESENT#2 | 10 | PRESENT#1 | 11 | ENABLE2# | 12 | ENABLE1# |
| 13 | PS_KILL2 | 14 | PS_KILL1 | 15 | THROTTLE#2 | 16 | THROTTLE#1 |
| 17 | FFS2# | 18 | FFS1# | 19 | AC/H/L2 | 20 | AC/H/L1 |
| 21 | EPOW#2 | 22 | EPOW#1 | 23 | NC | 24 | INTRUDER# |
| 25 | GND | 26 | GND | 27 | BP_SMBDAT | 28 | PS_SMBDAT |
| 29 | BP_SMBCLK | 30 | PS_SMBCLK | 31 | GND | 32 | PS_SMBALRT |
| 33 | SATARX2_P | 34 | PS_SMBRST | 35 | SATARX2_N | 36 | NC |
| 37 | GND | 38 | NC | 39 | GND | 40 | NC |
| 41 | SATATX2_N | 42 | NC | 43 | SATATX2_P | 44 | NC |
| 45 | GND | 46 | NC | 47 | GND | 48 | GND |
| 49 | SATARX1_P | 50 | Pair1_Fan1_Tach | 51 | SATARX1_N | 52 | Pair1_Fan1_PWM |
| 53 | GND | 54 | Pair1_Fan0_Tach | 55 | GND | 56 | Pair1_Fan0_PWM |
| 57 | SATATX1_N | 58 | Pair1_FFail# | 59 | SATATX1_P | 60 | GND |
| 61 | GND | 62 | Pair2_Fan1_Tach | 63 | GND | 64 | Pair2_Fan1_PWM |
| 65 | SATARX0_P | 66 | Pair2_Fan0_Tach | 67 | SATARX0_N | 68 | Pair2_Fan0_PWM |
| 69 | GND | 70 | Pair2_FFail# | 71 | GND | 72 | GND |
| 73 | SATATX0_N | 74 | Pair3_Fan1_Tach | 75 | SATATX0_P | 76 | Pair3_Fan1_PWM |
| 77 | GND | 78 | Pair3_Fan0_Tach | 79 | GND | 80 | Pair3_Fan0_PWM |
| 81 | NC | 82 | Pair3_FFail# | 83 | GND | 84 | GND |
| 85 | NC | 86 | Pair4_Fan1_Tach | 87 | NC | 88 | Pair4_Fan1_PWM |
| 89 | NC | 90 | Pair4_Fan0_Tach | 91 | GND | 92 | Pair4_Fan0_PWM |
| 93 | NC | 94 | Pair4_FFail# | 95 | NC | 96 | GND |
| 97 | NC | 98 | Pair5_Fan1_Tach | 99 | GND | 100 | Pair5_Fan1_PWM |
| 101 | NC | 102 | Pair5_Fan0_Tach | 103 | NC | 104 | Pair5_Fan0_PWM |
| 105 | FAULT# | 106 | Pair5_FFail# | 107 | GND | 108 | GND |
| 109 | USB1N | 110 | USB0P | 111 | USB1P | 112 | USB0N |
| 113 | USB1_PWR | 114 | USB0_PWR | 115 | GND | 116 | GND |
| 117 | GND | 118 | PWRGDLED# | 119 | RSTBTN | 120 | PWRBTN |

**P9** - **Power Supply Edge Card Connector**
60 position dual row connector, FOXCONN #E123093-5WAS-JF

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | 12V | 3 | 12V | 4 | 12V |
| 5 | 12V | 6 | 12V | 7 | 12V | 8 | 12V |
| 9 | GND | 10 | GND | 11 | GND | 12 | GND |
| 13 | GND | 14 | GND | 15 | GND | 16 | GND |
| 17 | GND | 18 | GND | 19 | 12Va | 20 | 12Va |
| 21 | GND | 22 | GND | 23 | GND | 24 | GND |
| 25 | GND | 26 | GND | 27 | GND | 28 | GND |
| 29 | 12V | 30 | 12V | 31 | 12V | 32 | 12V |
| 33 | 12V | 34 | 12V | 35 | 12V | 36 | 12V |

| Skt | Signal | Skt | Signal | Skt | Signal | Skt | Signal |
|---|---|---|---|---|---|---|---|
| 1 | NC | 2 | NC | 3 | VSENSE1_p | 4 | PS_KILL1 |
| 5 | NC | 6 | DC_GOOD1 | 7 | PRESENT1# | 8 | PS_SMB_ALRT# |
| 9 | NC | 10 | GND | 11 | PS_SMB_SDAT | 12 | PS_SMB_SCLK |
| 13 | PS_SMB_RESET# | 14 | Reserved | 15 | ADDRESS1 | 16 | Reserved |
| 17 | ENABLE1# | 18 | EPOW1# | 19 | FFS1# | 20 | THROTTLE1# |
| 21 | AC_H/L_1 | 22 | VSENSE1_n | 23 | NC | 24 | Reserved |

**Connectors** (continued)

**P10 - Power Supply Edge Card Connector**
60 position dual row connector, FOXCONN #E123093-5WAS-JF

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | 12V | 3 | 12V | 4 | 12V |
| 5 | 12V | 6 | 12V | 7 | 12V | 8 | 12V |
| 9 | GND | 10 | GND | 11 | GND | 12 | GND |
| 13 | GND | 14 | GND | 15 | GND | 16 | GND |
| 17 | GND | 18 | GND | 19 | 12Va | 20 | 12Va |
| 21 | GND | 22 | GND | 23 | GND | 24 | GND |
| 25 | GND | 26 | GND | 27 | GND | 28 | GND |
| 29 | 12V | 30 | 12V | 31 | 12V | 32 | 12V |
| 33 | 12V | 34 | 12V | 35 | 12V | 36 | 12V |

| Skt | Signal | Skt | Signal | Skt | Signal | Skt | Signal |
|---|---|---|---|---|---|---|---|
| 1 | NC | 2 | NC | 3 | VSENSE2_p | 4 | PS_KILL2 |
| 5 | NC | 6 | DC_GOOD2 | 7 | PRESENT2# | 8 | PS_SMB_ALRT# |
| 9 | NC | 10 | GND | 11 | PS_SMB_SDAT | 12 | PS_SMB_SCLK |
| 13 | PS_SMB_RESET# | 14 | NC | 15 | ADDRESS2 | 16 | NC |
| 17 | ENABLE2# | 18 | EPOW2# | 19 | FFS2# | 20 | THROTTLE2# |
| 21 | AC_H/L_2 | 22 | VSENSE2_n | 23 | NC | 24 | NC |

**P11 - Fan Status LED Connector**
10 pin single row header, Tyco (Amp) #1-640456-0

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | Pair1_FFail# | 2 | Pair1_LED_p | 3 | Pair2_FFail# | 4 | Pair2_LED_p |
| 5 | Pair3_FFail# | 6 | Pair3_LED_p | 7 | Pair4_FFail# | 8 | Pair4_LED_p |
| 9 | Pair5_FFail# | 10 | Pair5_LED_p | | | | |

**P14 - System Status LED Connector**
7 pin single row header, Tyco (Amp) #640456-7

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | GND | 2 | PWRGDLED# | 3 | RSTBTN | 4 | PWRBTN |
| 5 | VCC5 | 6 | FAULT# | 7 | VCC5 | | |

**P19 - I2C Header Connector – Not Populated**
3 pin single row header, Tyco (Amp) #640456-3

| Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|
| 1 | D | 2 | C | 3 | G |

**P22 - Dual Universal Serial Bus (USB) 2.0 Header**
10 pin dual row header, Amp #1761610-3
(+5V fused with self-resetting fuses)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V-USB12 | 2 | +5V-USB13 |
| 3 | USB12- | 4 | USB13- |
| 5 | USB12+ | 6 | USB13+ |
| 7 | GND-USB12 | 8 | GND-USB13 |
| 9 | Shield | 10 | Shield |

**P30 - Dual System Fan Assembly Connector – Fan Pair Number 5**
6 pin single row header, Molex #J-MLX-75730-0206

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | Pair5_Fan1_Tach | 3 | Pair5_Fan1_PWM | 4 | Pair5_Fan0_Tach |
| 5 | Pair5_Fan0_PWM | 6 | GND | | | | |

**P31 - Dual System Fan Assembly Connector – Fan Pair Number 4**

6 pin single row header, Molex #J-MLX-75730-0206

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | Pair4_Fan1_Tach | 3 | Pair4_Fan1_PWM | 4 | Pair4_Fan0_Tach |
| 5 | Pair4_Fan0_PWM | 6 | GND | | | | |

**P32 - Dual System Fan Assembly Connector – Fan Pair Number 3**

6 pin single row header, Molex #J-MLX-75730-0206

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | Pair3_Fan1_Tach | 3 | Pair3_Fan1_PWM | 4 | Pair3_Fan0_Tach |
| 5 | Pair3_Fan0_PWM | 6 | GND | | | | |

**P33 - Dual System Fan Assembly Connector – Fan Pair Number 2**

6 pin single row header, Molex #J-MLX-75730-0206

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | Pair2_Fan1_Tach | 3 | Pair2_Fan1_PWM | 4 | Pair2_Fan0_Tach |
| 5 | Pair2_Fan0_PWM | 6 | GND | | | | |

**P34 - Dual System Fan Assembly Connector – Fan Pair Number 1**

6 pin single row header, Molex #J-MLX-75730-0206

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | 12V | 2 | Pair1_Fan1_Tach | 3 | Pair1_Fan1_PWM | 4 | Pair1_Fan0_Tach |
| 5 | Pair1_Fan0_PWM | 6 | GND | | | | |

**P38 - Intrusion Alert Signal Connector**

2 pin single row header, Tyco (Amp) #640456-2

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GND | 2 | INTRUSION# |

# *Appendix A MBC8240 BIOS Messages*

**Introduction**
A status code is a data value used to indicate progress during the boot phase. These codes are outputted to I/O port 80h on the MBC8240 card. Aptio 4.x core outputs checkpoints throughout the boot process to indicate the task the system is currently executing. Status codes are very useful in aiding software developers or technicians in debugging problems that occur during the pre-boot process.

**Aptio Boot Flow**
While performing the functions of the traditional BIOS, Aptio 4.x core follows the firmware model described by the Intel Platform Innovation Framework for EFI ("the Framework"). The Framework refers the following "boot phases", which may apply to various status code descriptions:

- Security (SEC) – initial low-level initialization
- Pre-EFI Initialization (PEI) – memory initialization[1]
- Driver Execution Environment (DXE) – main hardware initialization[2]
- Boot Device Selection (BDS) – system setup, pre-OS user interface & selecting a bootable device (CD/DVD, HDD, USB, Network, Shell, …)

Analogous to "bootblock" functionality of legacy BIOS
[2] Analogous to "POST" functionality in legacy BIOS

**BIOS Beep Codes**
The Pre-EFI Initialization (PEI) and Driver Execution Environment (DXE) phases of the Aptio BIOS use audible beeps to indicate error codes. The number of beeps indicates specific error conditions.

**PEI Beep Codes**

| # of Beeps | Description |
|---|---|
| 1 | Memory not Installed |
| 1 | Memory was installed twice (InstallPeiMemory routine in PEI Core called twice) |
| 2 | Recovery started |
| 3 | DXEIPL was not found |
| 3 | DXE Core Firmware Volume was not found |
| 7 | Reset PPI is not available |
| 4 | Recovery failed |
| 4 | S3 Resume failed |

**DXE Beep Codes**

| # of Beeps | Description |
|---|---|
| 4 | Some of the Architectural Protocols are not available |
| 5 | No Console Output Devices are found |
| 5 | No Console Input Devices are found |
| 1 | Invalid password |
| 6 | Flash update is failed |
| 7 | Reset protocol is not available |
| 8 | Platform PCI resource requirements cannot be met |

**BIOS Status Codes**

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the CARD, just above the board's battery socket. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the MBC8240 CARD. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

The HEX to LED chart in the POST Code LEDs section will serve as a guide to interpreting specific BIOS status codes.

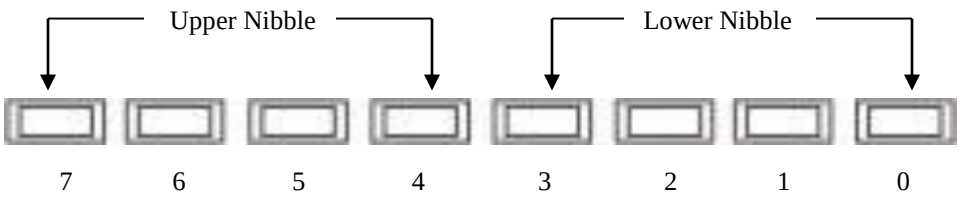
**BIOS Status POST Code LEDs**

As the POST (Power On Self Test) routines are performed during boot-up, test codes are displayed on Port 80 POST code LEDs 0, 1, 2, 3, 4, 5, 6 and 7. These LED are located on the top of the CARD, just above the board's SATA connectors and slightly toward the right. The POST Code LEDs and are numbered from right (position 1 = LED0) to left (position 8 – LED7).

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following chart is a key to interpreting the POST codes displayed on LEDs 0 through 7 on the MBC8240 CARD. Refer to the board layout in the *Specifications* chapter for the exact location of the POST code LEDs.

| Upper Nibble (UN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED7 | LED6 | LED5 | LED4 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |

| Lower Nibble (LN) | | | | |
|---|---|---|---|---|
| Hex. Value | LED3 | LED2 | LED1 | LED0 |
| 0 | Off | Off | Off | Off |
| 1 | Off | Off | Off | On |
| 2 | Off | Off | On | Off |
| 3 | Off | Off | On | On |
| 4 | Off | On | Off | Off |
| 5 | Off | On | Off | On |
| 6 | Off | On | On | Off |
| 7 | Off | On | On | On |
| 8 | On | Off | Off | Off |
| 9 | On | Off | Off | On |
| A | On | Off | On | Off |
| B | On | Off | On | On |
| C | On | On | Off | Off |
| D | On | On | Off | On |
| E | On | On | On | Off |
| F | On | On | On | On |




**MBC8240 POST Code LEDs**
(LED0 is located closest to the memory DIMM sockets)

**Status Code Ranges**

| Status Code Range | Description |
|---|---|
| 0x01 – 0x0F | SEC Status Codes & Errors |
| 0x10 – 0x2F | PEI execution up to and including memory detection |
| 0x30 – 0x4F | PEI execution after memory detection |
| 0x50 – 0x5F | PEI errors |
| 0x60 – 0xCF | DXE execution up to BDS |
| 0xD0 – 0xDF | DXE errors |
| 0xE0 – 0xE8 | S3 Resume (PEI) |
| 0xE9 – 0xEF | S3 Resume errors (PEI) |
| 0xF0 – 0xF8 | Recovery (PEI) |
| 0xF9 – 0xFF | Recovery errors (PEI) |

**SEC Status Codes**

| Status Code | Description |
|---|---|
| 0x0 | Not used |
| **Progress Codes** | |
| 0x1 | Power on. Reset type detection (soft/hard). |
| 0x2 | AP initialization before microcode loading |
| 0x3 | North Bridge initialization before microcode loading |
| 0x4 | South Bridge initialization before microcode loading |
| 0x5 | OEM initialization before microcode loading |
| 0x6 | Microcode loading |
| 0x7 | AP initialization after microcode loading |
| 0x8 | North Bridge initialization after microcode loading |
| 0x9 | South Bridge initialization after microcode loading |
| 0xA | OEM initialization after microcode loading |
| 0xB | Cache initialization |
| **SEC Error Codes** | |
| 0xC – 0xD | Reserved for future AMI SEC error codes |
| 0xE | Microcode not found |
| 0xF | Microcode not loaded |

**SEC Beep Codes**

There are no SEC Beep codes associated with this phase of the Aptio BIOS boot process.

**PEI Status Codes**

| Status Code | Description |
|---|---|
| **Progress Codes** | |
| 0x10 | PEI Core is started |
| 0x11 | Pre-memory CPU initialization is started |
| 0x12 | Pre-memory CPU initialization (CPU module specific) |
| 0x13 | Pre-memory CPU initialization (CPU module specific) |
| 0x14 | Pre-memory CPU initialization (CPU module specific) |
| 0x15 | Pre-memory North Bridge initialization is started |
| 0x16 | Pre-Memory North Bridge initialization (North Bridge module specific) |
| 0x17 | Pre-Memory North Bridge initialization (North Bridge module specific) |
| 0x18 | Pre-Memory North Bridge initialization (North Bridge module specific) |
| 0x19 | Pre-memory South Bridge initialization is started |
| 0x1A | Pre-memory South Bridge initialization (South Bridge module specific) |
| 0x1B | Pre-memory South Bridge initialization (South Bridge module specific) |
| 0x1C | Pre-memory South Bridge initialization (South Bridge module specific) |
| 0x1D – 0x2A | OEM pre-memory initialization codes |
| 0x2B | Memory initialization. Serial Presence Detect (SPD) data reading |
| 0x2C | Memory initialization. Memory presence detection |
| 0x2D | Memory initialization. Programming memory timing information |
| 0x2E | Memory initialization. Configuring memory |
| 0x2F | Memory initialization (other). |
| 0x30 | Reserved for ASL (see ASL Status Codes section below) |
| 0x31 | Memory Installed |
| 0x32 | CPU post-memory initialization is started |
| 0x33 | CPU post-memory initialization. Cache initialization |
| 0x34 | CPU post-memory initialization. Application Processor(s) (AP) initialization |
| 0x35 | CPU post-memory initialization. Boot Strap Processor (BSP) selection |
| 0x36 | CPU post-memory initialization. System Management Mode (SMM) initialization |
| 0x37 | Post-Memory North Bridge initialization is started |
| 0x38 | Post-Memory North Bridge initialization (North Bridge module specific) |
| 0x39 | Post-Memory North Bridge initialization (North Bridge module specific) |
| 0x3A | Post-Memory North Bridge initialization (North Bridge module specific) |
| 0x3B | Post-Memory South Bridge initialization is started |
| 0x3C | Post-Memory South Bridge initialization (South Bridge module specific) |
| 0x3D | Post-Memory South Bridge initialization (South Bridge module specific) |
| 0x3E | Post-Memory South Bridge initialization (South Bridge module specific) |
| 0x3F-0x4E | OEM post memory initialization codes |
| 0x4F | DXE IPL is started |
| | |

| **PEI Error Codes** | |
|---|---|
| 0x50 | Memory initialization error. Invalid memory type or incompatible memory speed |
| 0x51 | Memory initialization error. SPD reading has failed |
| 0x52 | Memory initialization error. Invalid memory size or memory modules do not match. |
| 0x53 | Memory initialization error. No usable memory detected |
| 0x54 | Unspecified memory initialization error. |
| 0x55 | Memory not installed |
| 0x56 | Invalid CPU type or Speed |
| 0x57 | CPU mismatch |
| 0x58 | CPU self test failed or possible CPU cache error |
| 0x59 | CPU micro-code is not found or micro-code update is failed |
| 0x5A | Internal CPU error |
| 0x5B | reset PPI is not available |
| 0x5C-0x5F | Reserved for future AMI error codes |
| **S3 Resume Progress Codes** | |
| 0xE0 | S3 Resume is stared (S3 Resume PPI is called by the DXE IPL) |
| 0xE1 | S3 Boot Script execution |
| 0xE2 | Video repost |
| 0xE3 | OS S3 wake vector call |
| 0xE4-0xE7 | Reserved for future AMI progress codes |
| 0xE0 | S3 Resume is stared (S3 Resume PPI is called by the DXE IPL) |
| **S3 Resume Error Codes** | |
| 0xE8 | S3 Resume Failed in PEI |
| 0xE9 | S3 Resume PPI not Found |
| 0xEA | S3 Resume Boot Script Error |
| 0xEB | S3 OS Wake Error |
| 0xEC-0xEF | Reserved for future AMI error codes |
| **Recovery Progress Codes** | |
| 0xF0 | Recovery condition triggered by firmware (Auto recovery) |
| 0xF1 | Recovery condition triggered by user (Forced recovery) |
| 0xF2 | Recovery process started |
| 0xF3 | Recovery firmware image is found |
| 0xF4 | Recovery firmware image is loaded |
| 0xF5-0xF7 | Reserved for future AMI progress codes |
| **Recovery Error Codes** | |
| 0xF8 | Recovery PPI is not available |
| 0xF9 | Recovery capsule is not found |
| 0xFA | Invalid recovery capsule |
| 0xFB – 0xFF | Reserved for future AMI error codes |

**PEI Beep Codes**

| # of Beeps | Description |
|---|---|
| 1 | Memory not Installed |
| 1 | Memory was installed twice (InstallPeiMemory routine in PEI Core called twice) |
| 2 | Recovery started |
| 3 | DXEIPL was not found |
| 3 | DXE Core Firmware Volume was not found |
| 7 | Reset PPI is not available |
| 4 | Recovery failed |
| 4 | S3 Resume failed |

**DXE Status Codes**

| Status Code | Description |
|---|---|
| 0x60 | DXE Core is started |
| 0x61 | NVRAM initialization |
| 0x62 | Installation of the South Bridge Runtime Services |
| 0x63 | CPU DXE initialization is started |
| 0x64 | CPU DXE initialization (CPU module specific) |
| 0x65 | CPU DXE initialization (CPU module specific) |
| 0x66 | CPU DXE initialization (CPU module specific) |
| 0x67 | CPU DXE initialization (CPU module specific) |
| 0x68 | PCI host bridge initialization |
| 0x69 | North Bridge DXE initialization is started |
| 0x6A | North Bridge DXE SMM initialization is started |
| 0x6B | North Bridge DXE initialization (North Bridge module specific) |
| 0x6C | North Bridge DXE initialization (North Bridge module specific) |
| 0x6D | North Bridge DXE initialization (North Bridge module specific) |
| 0x6E | North Bridge DXE initialization (North Bridge module specific) |
| 0x6F | North Bridge DXE initialization (North Bridge module specific) |
| 0x70 | South Bridge DXE initialization is started |
| 0x71 | South Bridge DXE SMM initialization is started |
| 0x72 | South Bridge devices initialization |
| 0x73 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x74 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x75 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x76 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x77 | South Bridge DXE Initialization (South Bridge module specific) |
| 0x78 | ACPI module initialization |
| 0x79 | CSM initialization |

| | |
|---|---|
| 0x7A – 0x7F | Reserved for future AMI DXE codes |
| 0x80 – 0x8F | OEM DXE initialization codes |
| 0x90 | Boot Device Selection (BDS) phase is started |
| 0x91 | Driver connecting is started |
| 0x92 | PCI Bus initialization is started |
| 0x93 | PCI Bus Hot Plug Controller Initialization |
| 0x94 | PCI Bus Enumeration |
| 0x95 | PCI Bus Request Resources |
| 0x96 | PCI Bus Assign Resources |
| 0x97 | Console Output devices connect |
| 0x98 | Console input devices connect |
| 0x99 | Super IO Initialization |
| 0x9A | USB initialization is started |
| 0x9B | USB Reset |
| 0x9C | USB Detect |
| 0x9D | USB Enable |
| 0x9E – 0x9F | Reserved for future AMI codes |
| 0xA0 | IDE initialization is started |
| 0xA1 | IDE Reset |
| 0xA2 | IDE Detect |
| 0xA3 | IDE Enable |
| 0xA4 | SCSI initialization is started |
| 0xA5 | SCSI Reset |
| 0xA6 | SCSI Detect |
| 0xA7 | SCSI Enable |
| 0xA8 | Setup Verifying Password |
| 0xA9 | Start of Setup |
| 0xAA | Reserved for ASL (see ASL Status Codes section below) |
| 0xAB | Setup Input Wait |
| 0xAC | Reserved for ASL (see ASL Status Codes section below) |
| 0xAD | Ready To Boot event |
| 0xAE | Legacy Boot event |
| 0xAF | Exit Boot Services event |
| 0xB0 | Runtime Set Virtual Address MAP Begin |
| 0xB1 | Runtime Set Virtual Address MAP End |
| 0xB2 | Legacy Option ROM Initialization |
| 0xB3 | System Reset |
| 0xB4 | USB hot plug |
| 0xB5 | PCI bus hot plug |
| 0xB6 | Clean-up of NVRAM |
| 0xB7 | Configuration Reset (reset of NVRAM settings) |

| | |
|---|---|
| 0xB8 – 0xBF | Reserved for future AMI codes |
| 0xC0 – 0xCF | OEM BDS initialization codes |
| **DXE Error Codes** | |
| 0xD0 | CPU initialization error |
| 0xD1 | North Bridge initialization error |
| 0xD2 | South Bridge initialization error |
| 0xD3 | Some of the Architectural Protocols are not available |
| 0xD4 | PCI resource allocation error. Out of Resources |
| 0xD5 | No Space for Legacy Option ROM |
| 0xD6 | No Console Output Devices are found |
| 0xD7 | No Console Input Devices are found |
| 0xD8 | Invalid password |
| 0xD9 | Error loading Boot Option (LoadImage returned error) |
| 0xDA | Boot Option is failed (StartImage returned error) |
| 0xDB | Flash update is failed |
| 0xDC | Reset protocol is not available |

**DXE Beep Codes**

| # of Beeps | Description |
|---|---|
| 4 | Some of the Architectural Protocols are not available |
| 5 | No Console Output Devices are found |
| 5 | No Console Input Devices are found |
| 1 | Invalid password |
| 6 | Flash update is failed |
| 7 | Reset protocol is not available |
| 8 | Platform PCI resource requirements cannot be met |

### ACPI/ASL Status Codes

| Status Code | Description |
|---|---|
| 0x01 | System is entering S1 sleep state |
| 0x02 | System is entering S2 sleep state |
| 0x03 | System is entering S3 sleep state |
| 0x04 | System is entering S4 sleep state |
| 0x05 | System is entering S5 sleep state |
| 0x10 | System is waking up from the S1 sleep state |
| 0x20 | System is waking up from the S2 sleep state |
| 0x30 | System is waking up from the S3 sleep state |
| 0x40 | System is waking up from the S4 sleep state |
| 0xAC | System has transitioned into ACPI mode. Interrupt controller is in PIC mode. |
| 0xAA | System has transitioned into ACPI mode. Interrupt controller is in APIC mode. |

### OEM-Reserved Status Code Ranges

| Status Code | Description |
|---|---|
| 0x5 | OEM SEC initialization before microcode loading |
| 0xA | OEM SEC initialization after microcode loading |
| 0x1D – 0x2A | OEM pre-memory initialization codes |
| 0x3F – 0x4E | OEM PEI post memory initialization codes |
| 0x80 – 0x8F | OEM DXE initialization codes |
| 0xC0 – 0xCF | OEM BDS initialization codes |